International Journal on Science and Technology (IJSAT)
E-ISSN: 2229-7677 ● Website: www.ijsat.org ● Email: editor@ijsat.org

Simulation of Self Balanced Switched Capacitor Based Thirteen Level Inverter

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Abstract

The designing of the thirteen level inverter based on switched capacitors with the ability of self-balancing is presented in this article. The proposed inverter converts the low DC voltage into high AC voltage by connecting the switched capacitors in series-parallel. The Phase Disposition modulation scheme with Multi-carrier is developed to generate the switching pulses. The capacitor voltages are balanced itself which improves the performance of the system. As opposite to existing switched-capacitor based inverters, the proposed inverters do not have an H-bridge circuit and the voltage stress of the switches is not exceeded to the supply voltage. The voltage ratings of each mode of operation is realized in mathematically and the harmonic distortions are also observed at different modulation indices. The MATLAB/SIMULINK is used to simulate the inverter and observed the advantages of low peak inverse voltage, total standing voltage, high conversion ability, and high boosting capability.

Keywords

Self-balanced, Switched Capacitor, Multi-carrier based Phase Disposition PWM, Thirteen level Boost inverter, Peak Inverse Voltage (PIV), Total Standing Voltage (TSV).

1. Introduction

The demand for quality and reliable power is increasing nowadays for domestic and industrial applications. Therefore, it is necessary to provide quality and reliable power for the utility grids. For uninterrupted power supplies, generally, inverters are preffered. The two level Inverters are not able to produce high voltages without disturbances like harmonics, switching losses. So, Multilevel Inverters are preferred to provide continuous and reliable power for industrial and applications. The advantages such as low voltage stress on the switches, low harmonic distortions, the resemblance of the quality sinusoidal waveform and operating with low switching frequency are increasing its popularity [1].

Multilevel Inverters are used almost in every electrical application such as HVDC applications, energy conversions, electrical vehicles, uninterruptible power supplies, etc. [4]. However, these multilevel inverters are also facing issues sch as high harmonic distortions, high switching and conduction losses. The boost converters, transformers and inductors are not required to boost the voltage in Multilevel Inverters. The inverter topology with H-bridge configuration has different blocking voltage of switches which results the high PIV and TSV. The asymmetric inverter topologies are restricted to certain voltage levels and for more levels the circuit will be complexity and expensive. The voltage balancing of capacitors plays an important role in Multilevel Inverter topologies. The Researchers are focussing on

novel topologies that lessen the problems associated with traditional MLIs.

The H-bridge configuration of five level inverter is connected to the utility grid with space vector modulation scheme in [11]. The author proposed single phase seven level inverter with three DC sources in [12]. The topology has auxillary circuit to produce seven level, H-Bridge circuit as main circuit which produces phase shift. The asymmetrical nine level inverter topology is presented in [13]. However, the circuit design and voltage balancing of capacitors is very complexity and difficult. The three capacitors are used The generalized structure of topology [14] has three DC sources with level shift modulation scheme produces the eleven level output.

The multilevel inverters along with switched capacitor is implementing from the past few years to overcome the issues of the existing inverters. The boosting capability of seven-level inverter along with switched-capacitor topology is discussed in [18-19]. The quadruple boosting ability nine-level switched-capacitor based inverter is presented in [20]. The 13-level inverter which is very expensive due to utilizing of four DC sources in [21]. The two DC sources, two capacitors, and few power switches to generate the 13 level inverter in [22]. The fifteen level inverter is discussed in [23] with four DC sources that lead to complexity and expense. The multiport switched-capacitor based multilevel inverter [24] with H-bridge connection which results high switching stress and total standing voltage.

2. Thirteen Level Inverter based on Switched Capacitor

The thirteen level inverter based on switched-capacitor consists of a cascaded connection of five modules, single DC source and five capacitors as shown in Figure.1. Each module comprises the five semi-conductor switches $S_{a1} - S_{a5}$.

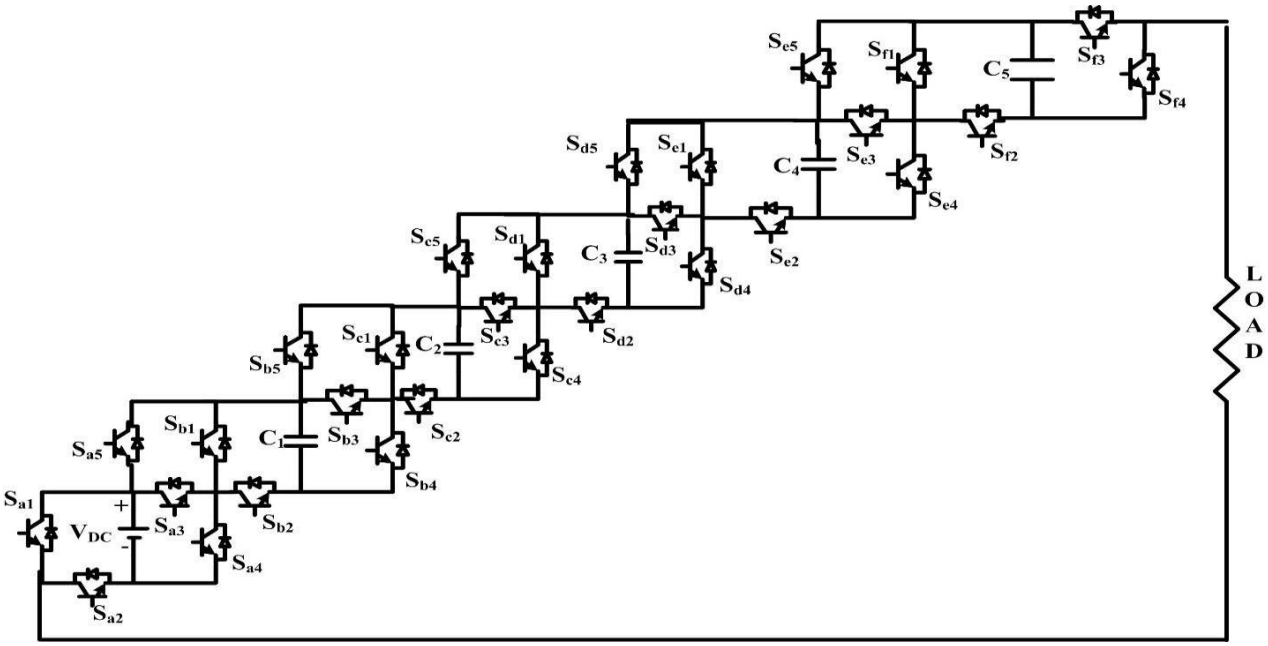

Figure.1: Thirteen level Inverter based on switched capacitor

The switches S_{a2} and S_{a5} are conducting to charge the capacitor by the parallel connection to the input DC source. By conducting the switches S_{a2} and S_{a3} will positively discharge the charged capacitor for $+V_{DC}$, the switches S_{a1} and S_{a4} are conducted to discharge negatively $-V_{DC}$. In order to match the input DC

voltage, the five capacitors are first completely charged and connected in parallel to the input DC source. The required staircase output will be produced by series discharging the charged capacitors at the selected switching frequency.

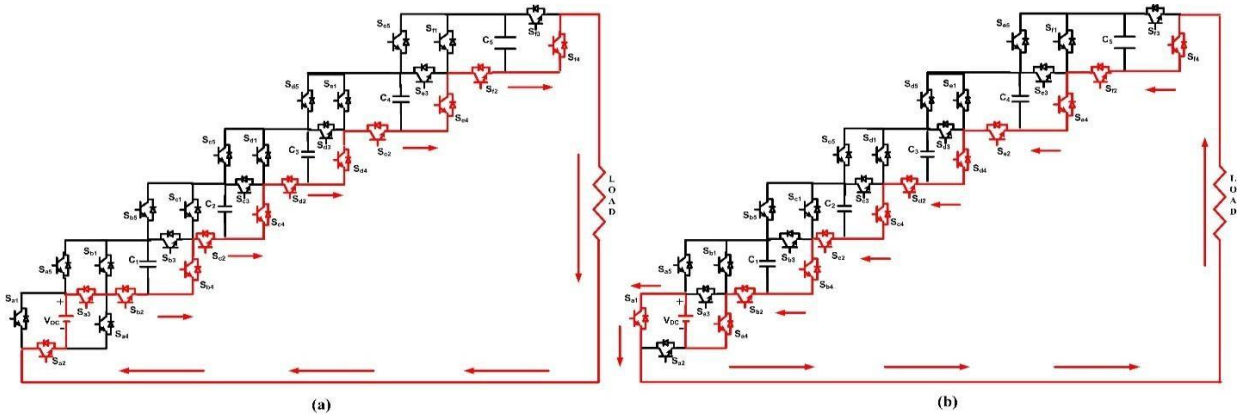

Figure.2: Modes of operation (a) +Vdc, (b) -Vdc

$V_0 = \pm V_{DC}$ **state**: For $\pm V_{DC}$ voltage level, the input DC source, seven switches, and five diodes will conduct. The switches S_{a3}, S_{b2}, S_{c2}, S_{d2}, S_{e2}, S_{f2}, S_{a2} are conducting along with the input DC voltage to obtain $+V_{DC}$ voltage as shown in Figure 2(a). Similarly, the switches S_{a1}, S_{f4}, S_{e4}, S_{d4}, S_{c4}, S_{b4}, S_{a4} will conduct to obtain $-V_{DC}$ voltage as represented in Figure 2(b).

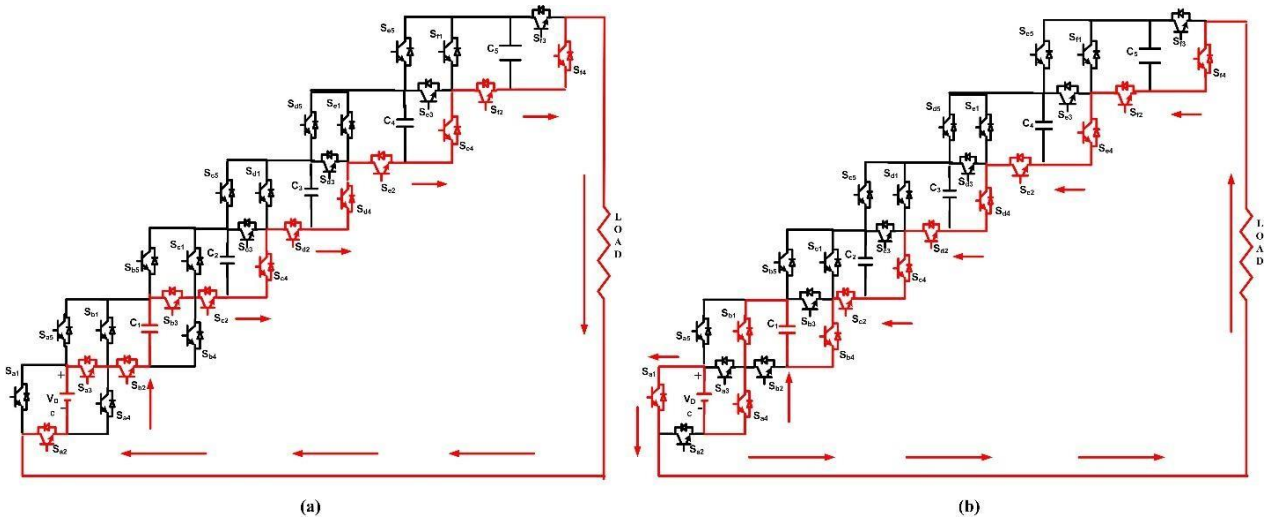

Figure 3: Modes of operation (a) +2Vdc, (b) -2Vdc

$V_0 = \pm 2V_{DC}$ **state:** The remaining capacitors, C_2 through C_5, are in parallel to the DC source in this state, while the capacitor C_1 is in series with the input DC source. The $2V_{DC}$ voltage is obtained by adding the capacitor voltage V_{C1} to the input voltage V_{in}. Figure 3(a) illustrates how the eight switches S_{a3}, S_{b2}, S_{b3}, S_{c2}, S_{d2}, S_{e2}, S_{f2}, S_{a2}, work in conduction to produce the $+2V_{DC}$ voltage level. Likewise, as seen in Figure 3(b), the switches S_{a1}, S_{f4}, S_{e4}, S_{d4}, S_{c4}, S_{b4}, S_{b1}, S_{a4} are operated to determine the $-2V_{DC}$ voltage level.

$$V_0 = V_{in} + V_{C1} = V_{DC} + V_{DC} = 2V_{DC} \qquad (1)$$

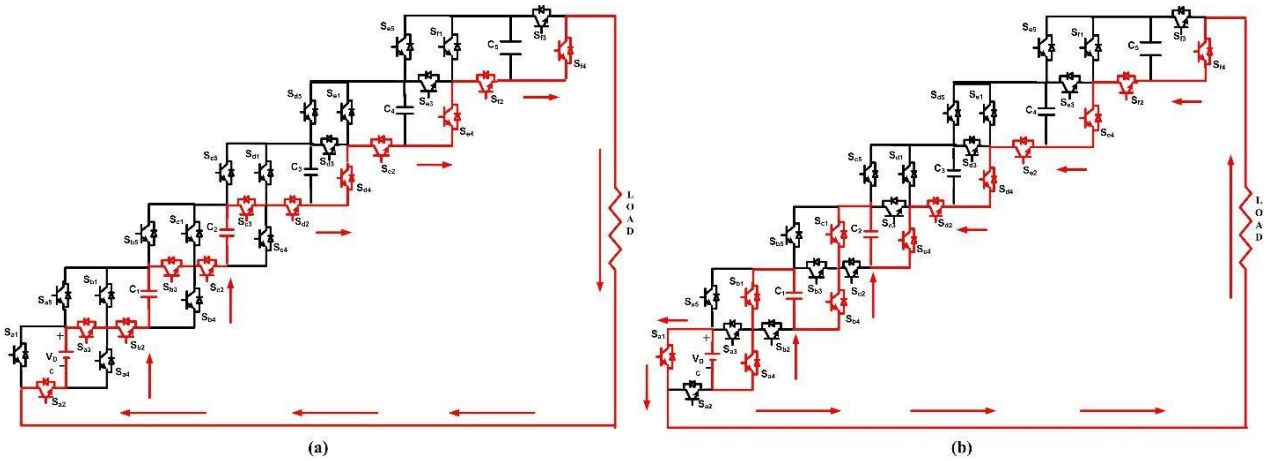

Figure 4: Modes of operation (a) +3Vdc, (b) -3Vdc

$V_0 = \pm 3V_{DC}$: The input DC source is connected to the capacitors $C_1 - C_2$ in series and $C_3 - C_5$ in parallel. In order to get the $3V_{DC}$ voltage in this state, the input voltage V_{in} is increased by the capacitor voltages V_{C1} and V_{C2}, and current flows through nine switches and three diodes. For $+3V_{DC}$, the switches S_{a3}, S_{b2}, S_{b3}, S_{c2}, S_{c3}, S_{d2}, S_{e2}, S_{f2}, S_{a2} will conduct as shown in Figure 4(a), and for $+3V_{DC}$, the switches S_{a1}, S_{f4}, S_{e4}, S_{d4}, S_{c4}, S_{c1}, S_{b4}, S_{b1}, S_{a4} are in ON state as presented in Figure 4(b).

$$V_0 = V_{in} + V_{C1} + V_{C2} = V_{DC} + V_{DC} + V_{DC} = 3V_{DC} \quad (2)$$

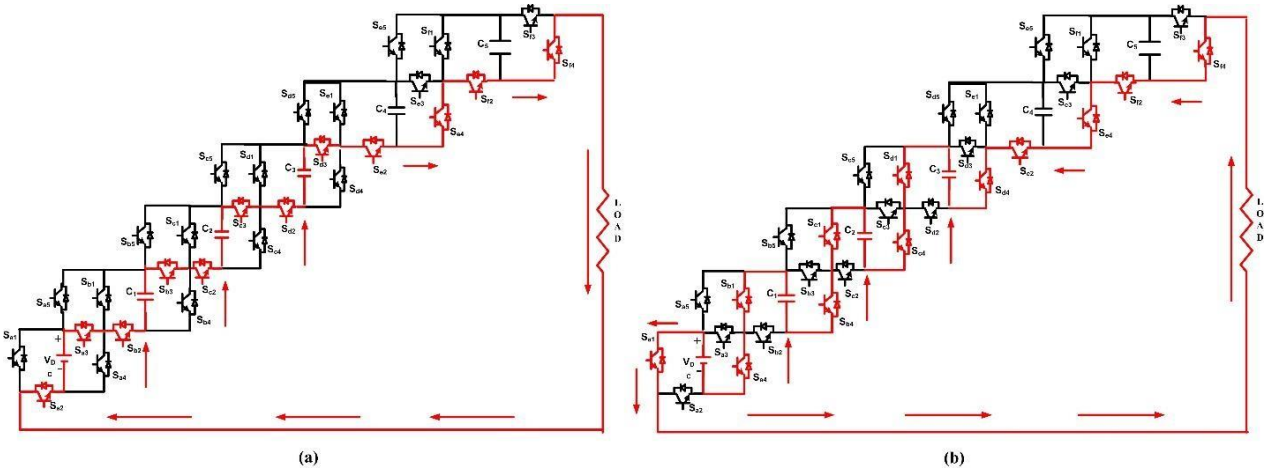

Figure 5: Modes of operation (a) +4Vdc, (b) -4Vdc

$V_0 = \pm 4V_{DC}$: To generate the $\pm 4V_{DC}$ level, the three capacitors $C_1 - C_3$ are connected in series with the input DC source to discharge the capacitor voltages through the ten switches and two diodes. At the same time, the remaining capacitors $C_4 - C_5$ is connected in parallel with DC source to charge the capacitors. The switches S_{a3}, S_{b2}, S_{b3}, S_{c2}, S_{c3}, S_{d2}, S_{d3}, S_{e2}, S_{f2}, S_{a2} will conduct for $+4V_{DC}$ as in Figure 5(a), and the switches S_{a1}, S_{f4}, S_{e4}, S_{d4}, S_{d1}, S_{c4}, S_{c1}, S_{b4}, S_{b1}, S_{a4} are in ON state to generate $-4V_{DC}$ as Figure 5(b).

$$V_0 = V_{in} + V_{C1} + V_{C2} + V_{C3} = V_{DC} + V_{DC} + V_{DC} + V_{DC} = 4V_{DC} \quad (3)$$

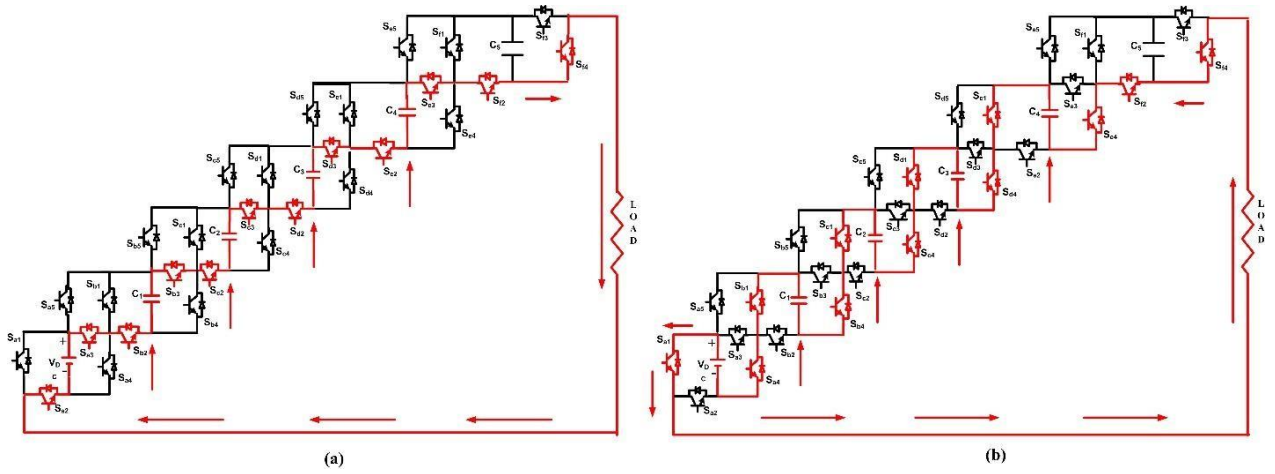

Figure 6: Modes of operation (a) +5Vdc, (b) -5Vdc

$V_0 = \pm 5V_{DC}$ **:** The capacitors $C_1 - C_4$ are connected in series and are discharged through the eleven switches S_{a3}, S_{b2}, S_{b3}, S_{c2}, S_{c3}, S_{d2}, S_{d3}, S_{e2}, S_{e3}, S_{f2}, S_{a2}, and a diode to produce $+5V_{DC}$ level as displayed in Figure 6(a). Similarly, the switches S_{a1}, S_{f4}, S_{e4}, S_{e1}, S_{d4}, S_{d1}, S_{c4}, S_{c1}, S_{b4}, S_{b1}, S_{a4} will conduct for $-5V_{DC}$ level as displayed in Figure 6(b).

$$V_0 = V_{in} + V_{C1} + V_{C2} + V_{C3} + V_{C4} = V_{DC} + V_{DC} + V_{DC} + V_{DC} + V_{DC} = 5V_{DC} \quad (4)$$

$V_0 = \pm 6V_{DC}$ **:** The five capacitors $C_1 - C_5$ completely discharges and combined with the input voltage to produce $6V_{DC}$ level. For $+6V_{DC}$, the switches S_{a3}, S_{b2}, S_{b3}, S_{c2}, S_{c3}, S_{d2}, S_{d3}, S_{e2}, S_{e3}, S_{f2}, S_{f3}, S_{a2} will conduct as shown in Figure 7(a). Similarly, for $-6V_{DC}$, the switches S_{a1}, S_{f4}, S_{f1}, S_{e4}, S_{e1}, S_{d4}, S_{d1}, S_{c4}, S_{c1}, S_{b4}, S_{b1}, S_{a4} will conducts as shown in Figure 7(b).

$$V_0 = V_{in} + V_{C1} + V_{C2} + V_{C3} + V_{C4} + V_{C5} = V_{DC} + V_{DC} + V_{DC} + V_{DC} + V_{DC} + V_{DC} = 6V_{DC}$$

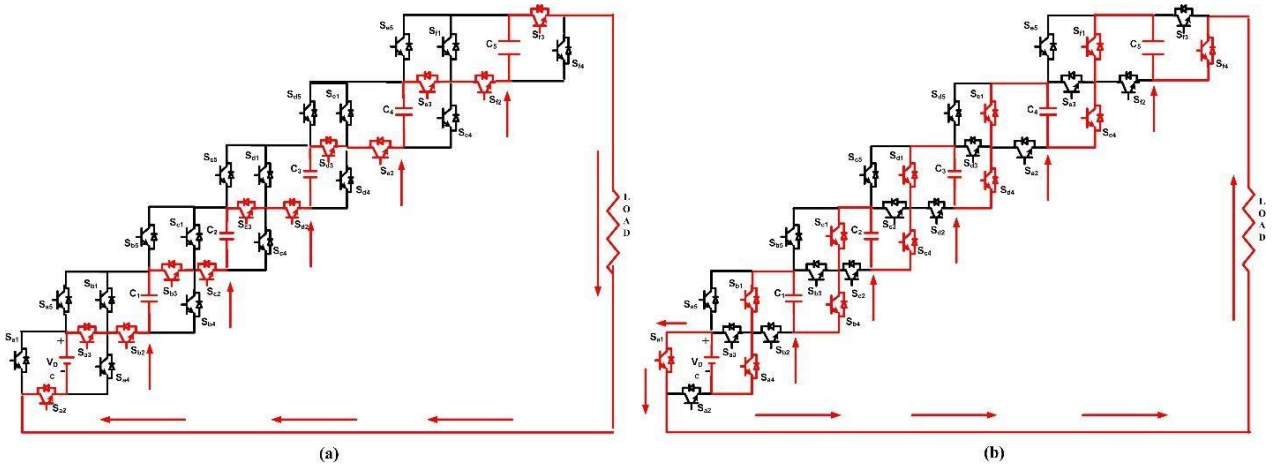

Figure 7: Modes of operation (a) +6Vdc,b) -6Vdc

Table 1. Positions of switches, diodes, and capacitors for each level.

Desired Level	Operating Switches	Operating Diodes	Capacitors State				
			C_1	C_2	C_3	C_4	C_5
$+V_{dc}$	S_{a3}, S_{b2}, S_{c2}, S_{d2}, S_{e2}, S_{f2}, S_{a2}	S_{b4}, S_{c4}, S_{d4}, S_{e4}, S_{f4}	↑	↑	↑	↑	↑
$+2V_{dc}$	S_{a3}, S_{b2}, S_{b3}, S_{c2}, S_{d2}, S_{e2}, S_{f2}, S_{a2}	S_{c4}, S_{d4}, S_{e4}, S_{f4}	↓	↑	↑	↑	↑
$+3V_{dc}$	S_{a3}, S_{b2}, S_{b3}, S_{c2}, S_{c3}, S_{d2}, S_{e2}, S_{f2}, S_{a2}	S_{d4}, S_{e4}, S_{f4}	↓	↓	↑	↑	↑
$+4V_{dc}$	S_{a3}, S_{b2}, S_{b3}, S_{c2}, S_{c3}, S_{d2}, S_{d3}, S_{e2}, S_{f2}, S_{a2}	S_{e4}, S_{f4}	↓	↓	↓	↑	↑
$+5V_{dc}$	S_{a3}, S_{b2}, S_{b3}, S_{c2}, S_{c3}, S_{d2}, S_{d3}, S_{e2}, S_{e3}, S_{f2}, S_{a2}	S_{f4}	↓	↓	↓	↓	↑
$+6V_{dc}$	S_{a3}, S_{b2}, S_{b3}, S_{c2}, S_{c3}, S_{d2}, S_{d3}, S_{e2}, S_{e3}, S_{f2}, S_{f3}, S_{a2}	----------	↓	↓	↓	↓	↓
$-6V_{dc}$	S_{a1}, S_{f4}, S_{f1}, S_{e4}, S_{e1}, S_{d4}, S_{d1}, S_{c4}, S_{c1}, S_{b4}, S_{b1}, S_{a4}	----------	↓	↓	↓	↓	↓
$-5V_{dc}$	S_{a1}, S_{f4}, S_{e4}, S_{e1}, S_{d4}, S_{d1}, S_{c4}, S_{c1}, S_{b4}, S_{b1}, S_{a4}	S_{f2}	↓	↓	↓	↓	↑
$-4V_{dc}$	S_{a1}, S_{f4}, S_{e4}, S_{d4}, S_{d1}, S_{c4}, S_{c1}, S_{b4}, S_{b1}, S_{a4}	S_{f2}, S_{e2},	↓	↓	↓	↑	↑
$-3V_{dc}$	S_{a1}, S_{f4}, S_{e4}, S_{d4}, S_{c4}, S_{c1}, S_{b4}, S_{b1}, S_{a4}	S_{f2}, S_{e2}, S_{d2}	↓	↓	↑	↑	↑
$-2V_{dc}$	S_{a1}, S_{f4}, S_{e4}, S_{d4}, S_{c4}, S_{b4}, S_{b1}, S_{a4}	S_{f2}, S_{e2}, S_{d2}, S_{c2}	↓	↑	↑	↑	↑
$-V_{dc}$	S_{a1}, S_{f4}, S_{e4}, S_{d4}, S_{c4}, S_{b4}, S_{a4}	S_{f2}, S_{e2}, S_{d2}, S_{c2}, S_{b2}	↑	↑	↑	↑	↑
↑ = Charging ; ↓ = Discharging							

4. Results and Discussion

The MATLAB/SIMULINK software is used to implement the thirteen-level inverter based on switched capacitors. The Switched Capacitors have the ability to sustained the voltage V_{DC}. The multicarrier

signals have frequency of 20KHZ are matched with the Sinusoidal reference signal of 50Hz to generate the switching pulses of the proposed inverter as shown in Figure 8.

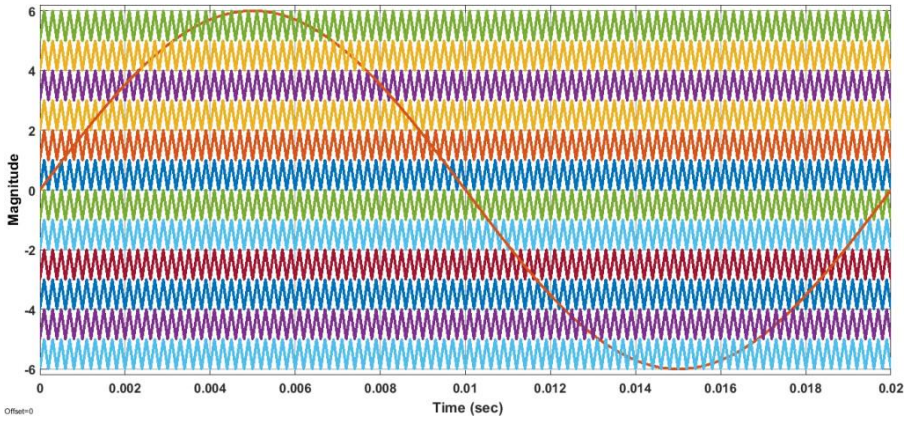

Figure 8 : Waveform of Phase Disposition Modulation

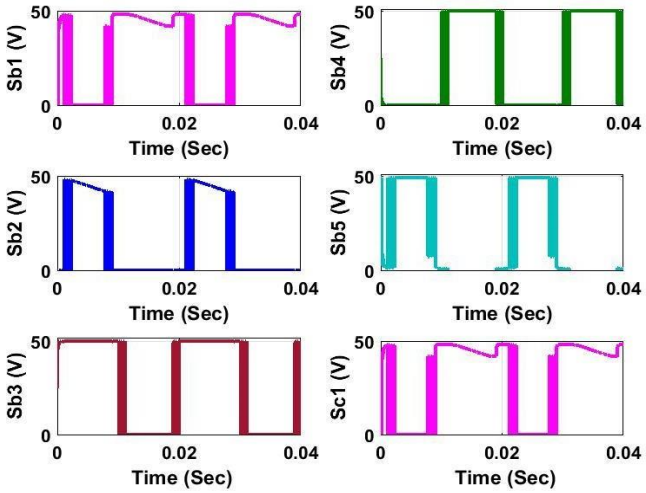

Figure 9: Withstanding voltages of Switches

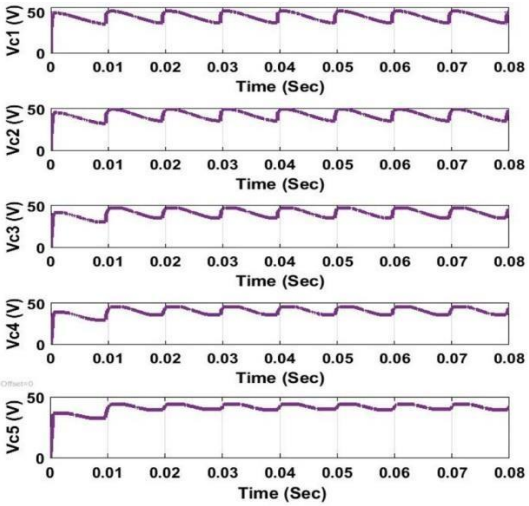

Figure 10: Voltage across capacitors during charging and discharging.

The thirteen-level output is obtained by applying the generated switching pulses to the inverter. The switches have the ability to sustained the voltage throughout the turn-on and off process. Furthermore, the

sustained voltage of each switch is same as applied voltage of 50V as displayed in Figure 9. The self-balancing technique is used to charge and discharge the switched capacitors. As illustrated in Figure 10, each capacitor discharges a 50V voltage when connected in series with the input DC voltage.

Table 2. Specifications.

Terms	**Ratings**
Applied Voltage (V_{DC})	50V
Desired voltage	250V
Switched Capacitors	5
Boosting Capability	5 Times
Peak Inverse Voltage (PIV)	$1V_{DC}$
Switches used	29
Sustained voltage of each switch	V_{DC}
Switching Frequency	20 KHz
Obtained output levels	13
Output Current	4.8 A
Resistor	50Ω
Inductor	10mH
Total Standing Voltage (TSV)	$5V_{DC}$

As seen in Figure 11, this suggested inverter generated thirteen levels of output of 250V and 4.8A respectively, with the application of 50V, the frequency and capacitor are being 50Hz and 1000μF to the load at modulation index MI = 1.

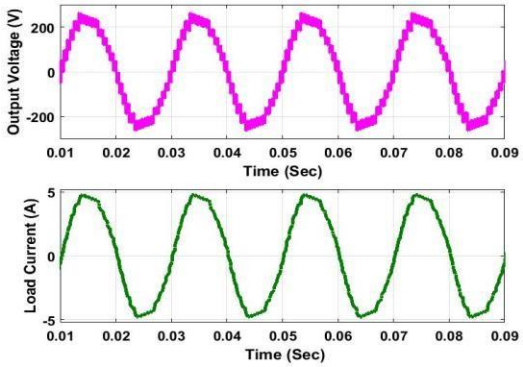

Figure 11: Performance of inverter at MI = 1.

As shown in Figure 12, this suggested inverter generated eleven levels of 210V and 3.9A respectively, with the applied voltage of 50V, the frequency and capacitor are being 50Hz and 1000μF to the load at modulation index MI = 0.7

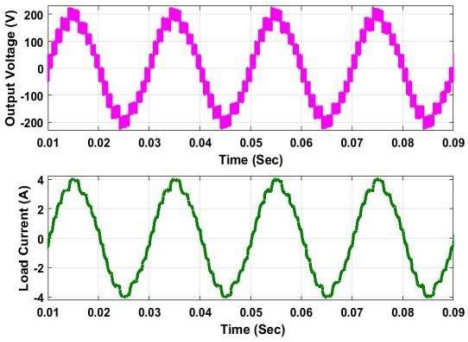

Figure 12 : Performance of inverter at MI = 0.7.

From the Figure 13, this suggested inverter generated seven levels of output of 140V and 2.4A respectively, with the applied voltage of 50V, the frequency and capacitor are being 50Hz and 1000µF to the load at modulation index MI = 0.5.

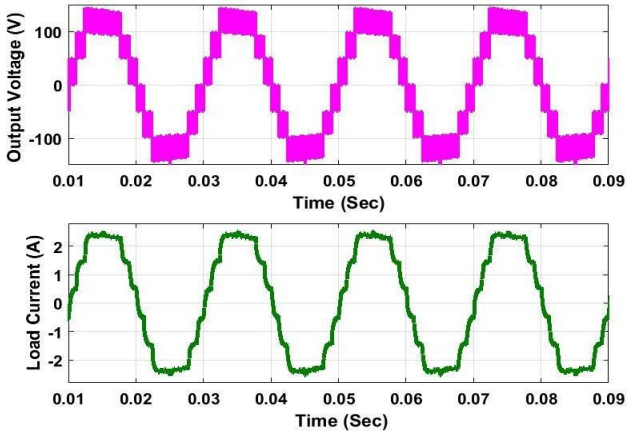

Figure 13: Performance of inverter at MI = 0.5.

The harmonic distortion analysis of proposed thirteen level inverter at different modulation indices are displayed in Figure 14, 15 and 16.

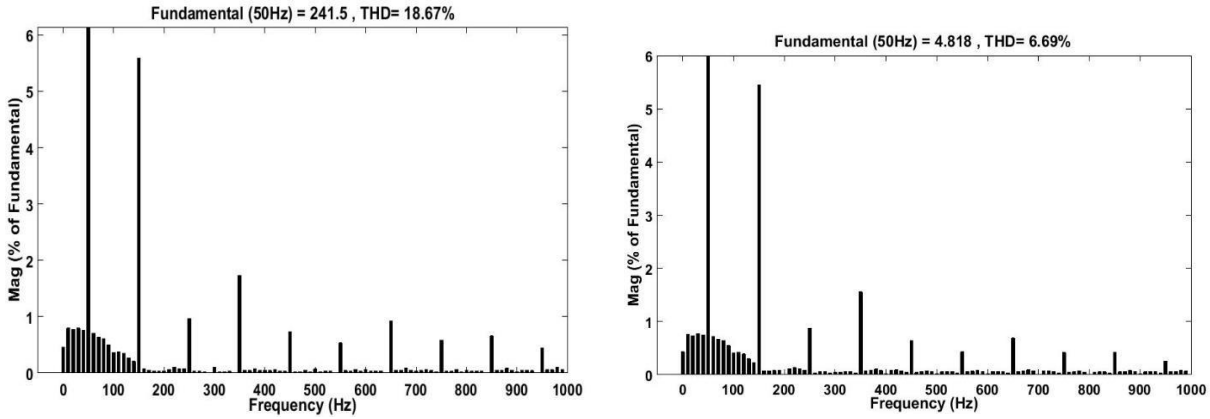

Figure 14: Analysis of THD at MI = 1.

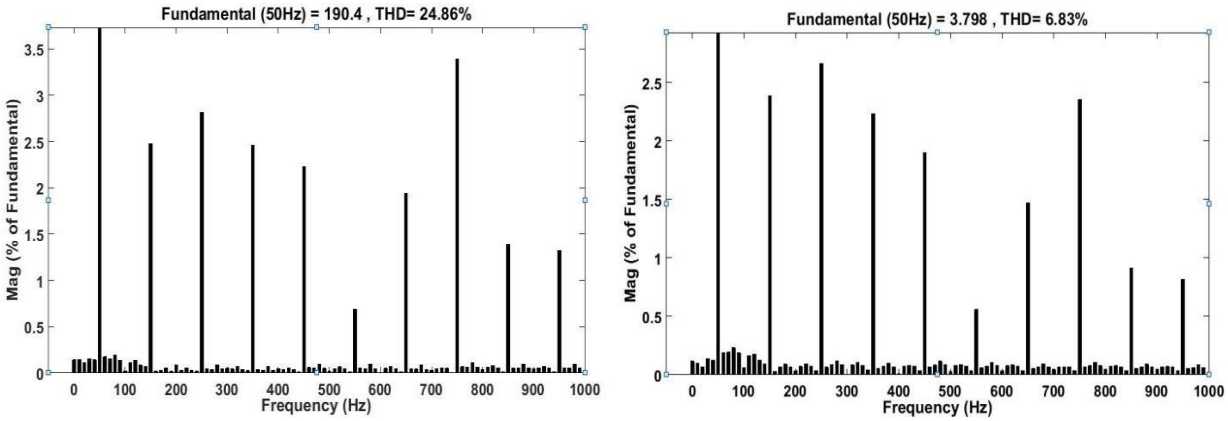

Figure 15: Analysis of THD at MI = 0.7.

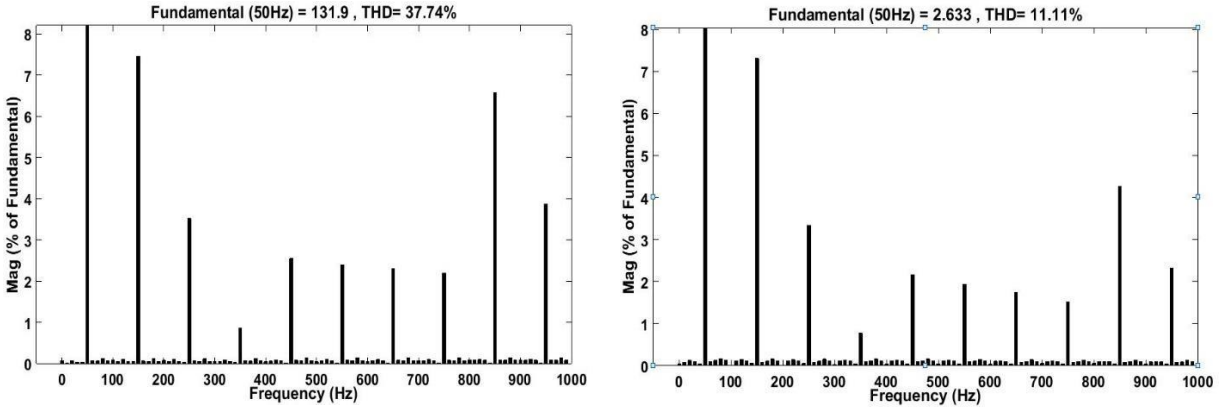

Fig.16: Analysis of THD at MI = 0.5.

5. Conclusion

The new assembly of thirteen level multilevel inverters is presented and simulated in this article. The proposed inverter converts the DC – AC by employing a single DC source and achieves the high boosting capability using switched capacitor technique. The detailed modes of operation is discussed. The capacitor voltages are balanced itself by using multi-carrier based phase disposition PWM control scheme. The switches are operated at the same frequency which results in the low conduction and switching losses. Due to not having an H-bridge circuit in the proposed inverter, the voltage stress of the switches is equal to V_{DC} which results in the low PIV and TSV.. Finally, for various modulation indexes, the simulation results demonstrate the feasibility and competence of the inverter.

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