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ANALYSIS AND IMPLEMENTATION OF LOW POWER TECHNIQUES IN VITERBI DECODER DESIGN

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Abstract:
Rapid developments in the field of wireless communication have created a rising demand for Viterbi decoder with long battery life, low power dissipation and low weight. Despite the significant progress in the last decade, the problems of power dissipation in the Viterbi decoder still remains challenging and require further technical solutions. Hence this research focuses on designing low power VLSI (Very Large Scale Integration) architectures for the Viterbi decoder for a constraint length of K=3 and discuss their performances in terms of power, speed and area. The convolutional encoders are designed for constraint length of K=3 to7. Thus the performance of the Viterbi decoder is improved by low power VLSI techniques. In order to reduce the power consumption and to increase the speed of the Viterbi decoder repeated iterations are performed at the same clock transition by unfolding algorithm. This unfolding algorithm is applied at the bit level to generate digit-serial architecture, which processes multiple words per clock cycle. The obtained results are compared with the existing 2 bit level pipe lined look ahead technique. It is observed that the proposed method reduced power consumption by 25.76% with 10.09% increase in speed. The limitation of this method is addressed by wave pipe lining technique and it is implemented to increase the speed of the architecture as the idle time of the non critical paths is reduced.The combined technique of Self Reset Logic (SRL) with wave pipe lining is used to design the architecture for the Viterbi decoder to reduce the power dissipation. Power consumption of the wave pipelining work is reduced by a factor of 72.31% when compared to the existing single rail domino logic. The area of the decoder increases with respect to its advantage of increase in speed.VLSI architecture for a Viterbi decoder based on GDI (Gate Diffusion Input) is designed to minimize the number of transistors and transitions. Thus the problem of high gate density in SRL based design is addressed by the GDI approach. GDI method yielded better results when compared to the average power consumption of Viterbi decoder with that of CMOS logic. Power consumption is reduced by 29%, for a frequency of 25 MHz and the area is reduced by 66%.Most of the decoders designed and fabricated today are synchronous. The problem of clock skew is a major challenge in the synchronous design. Alternatively, asynchronous systems are becoming familiar as they are not in need of global clock, as these systems are locally synchronized by means of communication protocols. Asynchronous VLSI architecture for a Viterbi decoder is designed using Quasi Delay Insensitive (QDI) templates and Differential Cascode Voltage Switch Logic (DCVSL). The performance of the asynchronous Viterbi decoder showed 56.20% less power consumption and has a frequency of 425 MHz when compared to that of synchronous design

Keywords: LOW POWER, DECODER.

1. INTRODUCTION

In the modern era, wireless communication technologies have advanced from cellular networks to satellite systems. Information coding theory plays a vital role in all these digital wireless communication systems, in order to achieve high efficiency and accuracy of the transmitting data, voice and image. A widely used error correction technique in the wireless communication systems is the channel coding. In channel coding, convolutional codes are commonly used for the transmission of data over a noisy channel. In decoding the convolutional codes at the receiver end, the Viterbi algorithm is found to be function efficiently in atmost all the wireless communication systems. Viterbi algorithm in its implementation is commonly known to be the Viterbi decoder.Viterbi decoder suits the best decoder for convolutional codes because of its fixed decoding time. Also recently Viterbi decoder finds its implementation in Very Large Scale Integration (VLSI) design. Minimization of power consumption and reduction of computational complexity of the Viterbi decoder in VLSI technology is a challenging problem for the researchers. The motivation for low power has been derived from the needs to reduce the power consumption, increase the speed and to reduce the weight. Thus the above factors stimulated the author to do research in this area.

2. LITERATURE SURVEY

1. The Viterbi algorithm proposed by Viterbi (1967, 1971) is widely used in digital communication. This method is efficient for the realization of maximum likelihood decoding of convolutional codes. Ajay Dholakia (1994) proved that the convolutional code finds its impact in encoding, error correction and decoding applications.
2. The research activities in the Viterbi decoder are categorized in two groups. The first group is based on altering the decoder architecture to obtain desired metrics, while the second group utilized different circuit implementation techniques to optimize the related metric
3. Chi-Ying Tsui et al. (1999) also made certain modifications in the ACS unit. Branch values were computed and a look up table was formed for the branch values. Operations in ACS unit were reduced by minimizing the number of comparators to six instead of nine
4. Bogdan et al. (2000) discussed precomputational architecture to reduce the power consumption of the ACS unit. Transistor level implementation in the precomputation portion of ACS unit was done with Single ended Pass transistor Logic (SPL). Yet, the limitation of SPL logic is that logic restoration cannot be maintained

3.DESIGN OF CONVOLUTIONAL ENCODER AND IMPLEMENTATION OF VITERBI DECODER

Convolutional codes are usually described using two parameters, namely the code rate and the constraint length. The code rate $r = k / n$, is expressed as a ratio of the number of bits into the convolutional encoder (k) to the number of channel symbols output by the convolutional encoder (n) in a given encoder cycle. The constraint length parameter K denotes the length of the convolutional encoder and it indicates how many k-bit stages are available to feed the combinational logic that produces the output symbols.

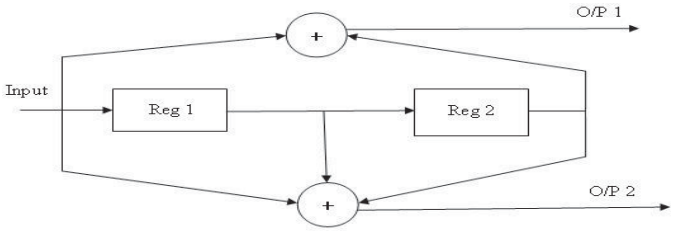

Figure 2.1 Convolutional Encoder for Code Rate ½ and Constraint Length *K*=3

State Diagram Representation for (2, 1, 3) Code

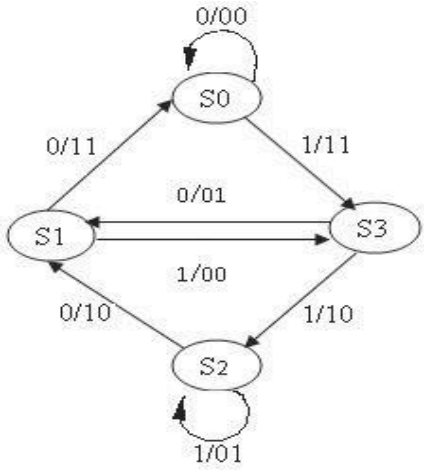

Figure 2.2 State Diagram for (2, 1, 3) Code

Tree Diagram Representation for (2, 1, 3) Code

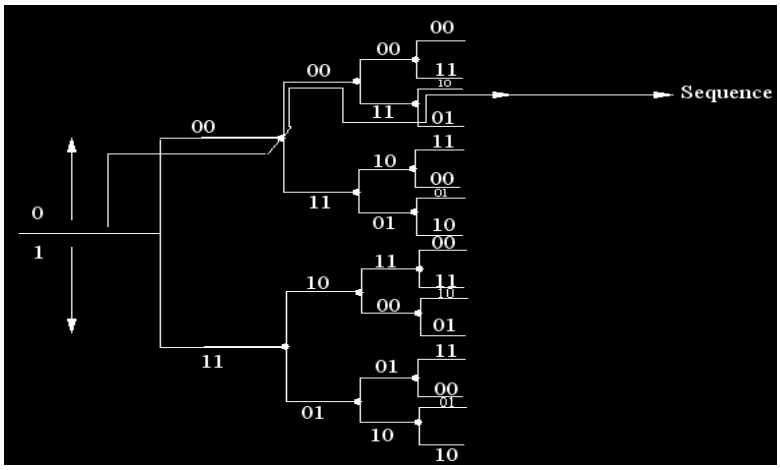

Figure 2.3 Tree Diagram for (2, 1, 3) Code

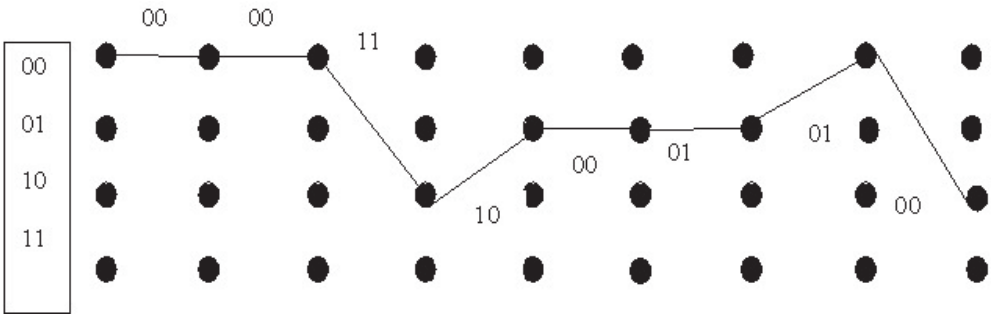

Figure 2.5 Trellis Diagram for the Encoder Sequence

Implementation Of The Viterbi Algorithm In The Proposed Methods

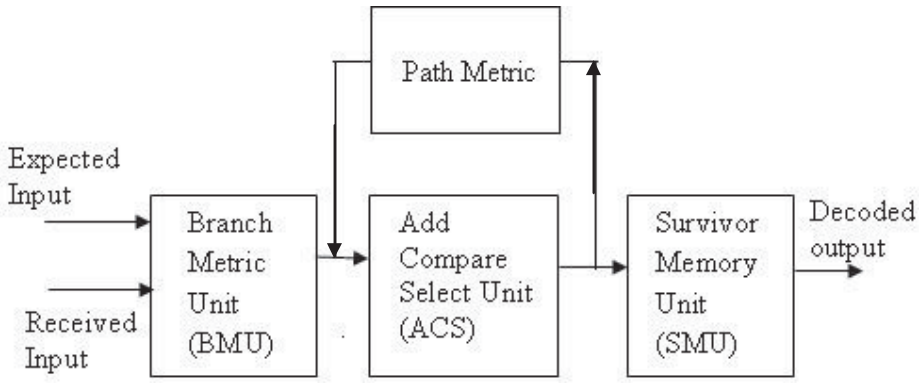

Figure 2.10 Block Diagram of the Viterbi Decoder

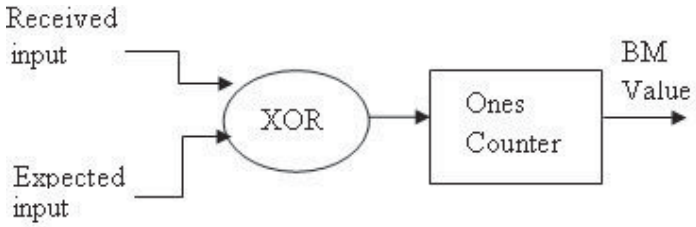

Figure 2.11 BMU for One State

Design Parameters Considered for Simulation

Viterbi decoder using the proposed four methods are designed for a constraint length of K=3 with a code rate of ½. Performance metrics like area, power and speed are evaluated by applying set of inputs to the Viterbi decoder (K=3) obtained from various constraint lengths of the encoder K=3 to 7. Literature survey indicates that the practical applications of Viterbi decoder involves constraint length from K=3 to 7. Input data are randomly given for the design. For each constraint length, a sample of 5 sets of 8 bit data is given as input to the decoder (which is the output of the encoder). The internal circuitry of the encoder changes for each constraint length, thus a unique input for all constraint length (K=3, 4, 5, 6 and 7) gives different outputs. Consequently, there is a constant variation in the power analysis result of the Viterbi decoder. In the proposed designs, the output value of the Viterbi decoder comprises errors, as it is the nature of the Viterbi decoder. The focus of the research is on low power and hence, concentration is not in the bit error rate analysis of the decoder.

Dataflow Graph Representations And Digit Serial Architecture For BMU

Unfolding concept is demonstrated with the help of dataflow graph. In dataflow graph depictions, the nodes represent computations (function or subtasks), the directed edges represent data paths (communications between nodes) and each edge U, V is assumed zero number of delays associated with it. Processing node is named as A; it can be a XOR gate, adder etc. Figure 3.2 shows the Dataflow graph for XOR gate

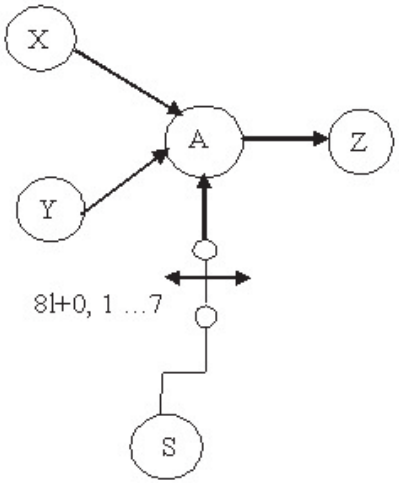

Figure 3.2 Dataflow Graph for XOR Gate

DIGIT SERIAL ACS UNIT

ACS unit consists of adder, comparator and selector. Digit serial architecture of a full adder with unfolding factor J=2 is illustrated in Figure 3.4. The word length becomes half of the original value as it is unfolded by 2. Inputs bm1 (0), pm1 (0), bm1 (1),…, pm1 (3) are fed as digit by digit to the adder in the first clock cycle. Adder outputs S0, S2 are obtained at 2l+0 switching instance and S1, S3 are obtained at the switching instance 2l+1. This process requires 2 clock cycles to obtain the output from the adder section.

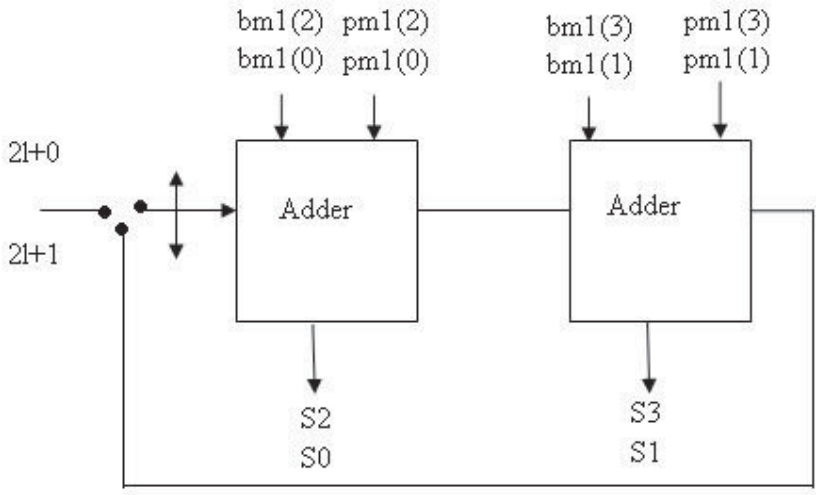

Figure 3.4 Digit Serial Architecture of a Full Adder with Unfolding Factor J=2

DESIGN OF SMU

The four states of the trellis are implemented in the SMU with 4*4 shift registers. For convenience the RTL view of 1* 4 SMU (one stage) is shown in Figure 3.6. In that, X and Y represent the sequences of the input for the multiplexer in the selector unit. The selector unit multiplexer is connected to the shift registers. The decision signal dec is fed from the ACS unit of the comparator. If the value of the dec is 1, then the minimum PM is decoded and stored in the register bit by bit. clkm, clks are used for shifting of bit in the registers

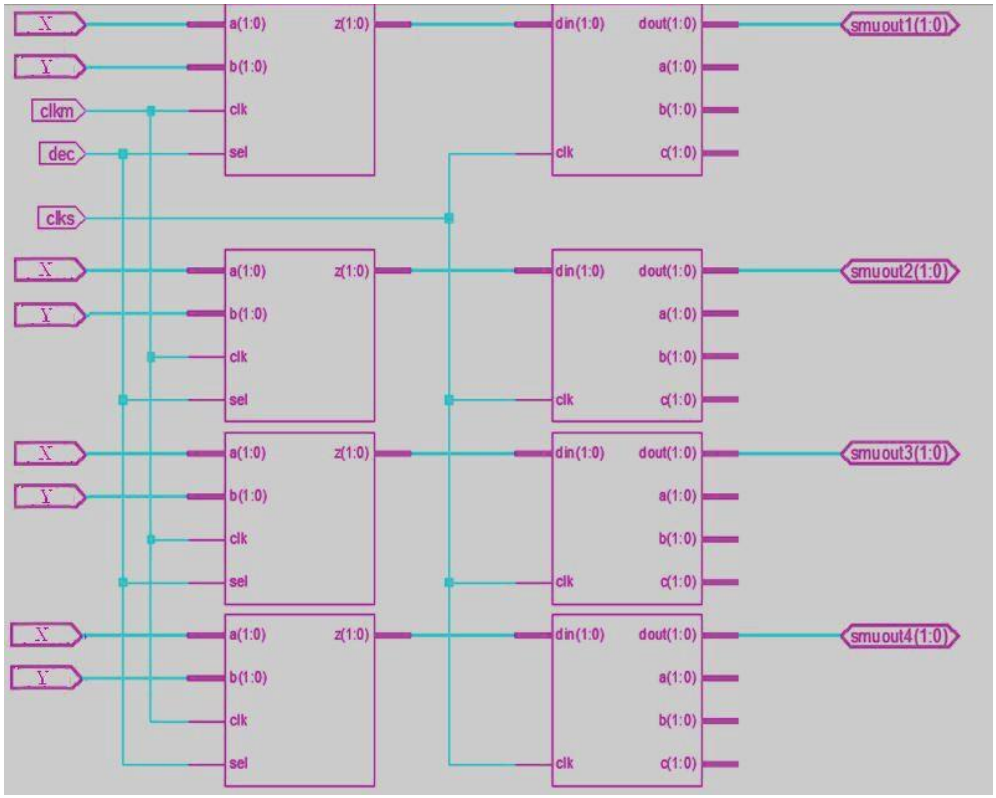

Figure 3.6 RTL View of 1* 4 SMU (one stage)

4.SIMULATION RESULTS

Output Waveform of Digit Serial BMU

The simulation output waveform of digit serial unfolded BMU is provided in Figure 3.7.

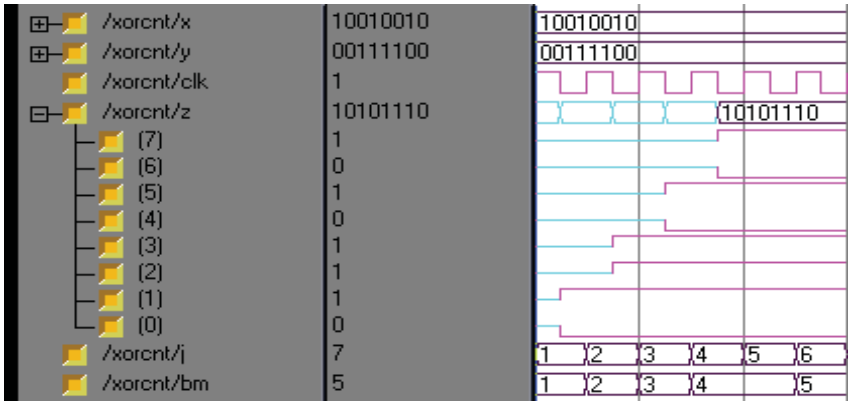

Figure 3.7 Output Waveform of Digit Serial Unfolded BMU

The inputs of BMU are X=10010010, Y=00111100 and a clock signal. The output of XOR gate is Z=10101110 and it is given to the counter. These counter counts the number of one present in the output of the XOR gate at 4 clock pulses. The counter output is the BM value of the particular path. The output value is BM=5.

Output Waveform of Digit Serial ACS Unit

The output waveform of digit serial ACS unit is given in Figure 3.8. The first adder inputs are bm1=0001, pm1=0001.The second adder inputs are bm2=1000, pm2=1000. The clock signal is given to the latch REG2. The sum of adder1 S=00010 and adder2 sum=10000.

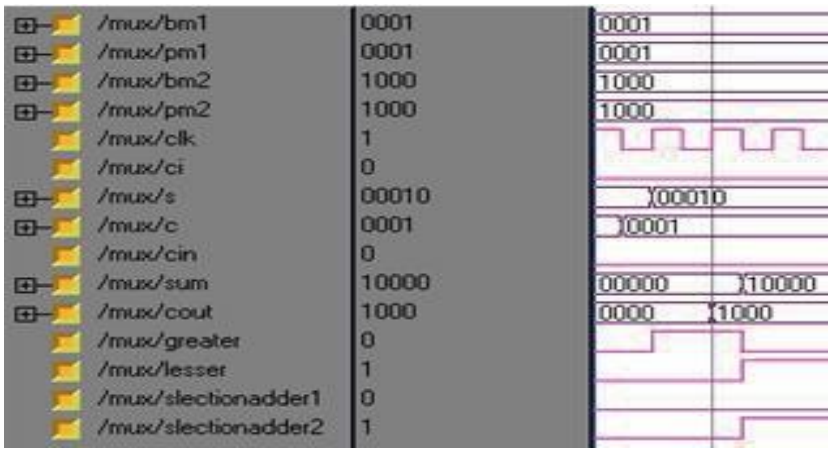

Figure 3.8 Output Waveform of Digit Serial ACS Unit

Output of Proposed Bit-Level Pipelined Viterbi Decoder

The simulated output waveform of bit-level pipelined Viterbi decoder is exhibited in Figure 3.9. Original message sequence is an 8 bit word. The output of the encoder is given to the input of the decoders. For convenience the entire process for 8 bit data is explained. In BM1 the received sequence X =11111101 and expected sequence Y =11111110. In BM2, the received sequence X1 =10001100 and expected sequence Y1
=10001110. The outputs of the BM unit are bm1=0010, bm2=0001. The output of the BMU is given to the ACS unit.

The input of the upper branch adder is (bm04) bm1=0010, pm1=0000, and input of lower branch adder is (bm14) bm2=0001, pm2=0000. The sum of upper branch adder is 0010 and sum of lower branch adder is 0001. The output of the two adders is given to the comparator and the selector. Based on the minimum value of the selector, the decoded sequence is recorded in the registers. The decoded sequence is thus obtained as 1111.

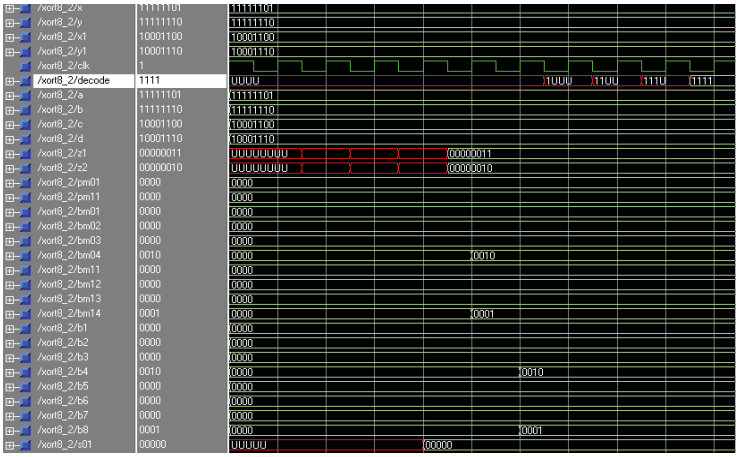

Figure 3.9 Output of Bit-Level Pipelined Viterbi Decoder

Performance Comparison of Viterbi Decoder in Terms of Power and Speed

Module Name	Existing 2 Bit Level Pipelined Viterbi Decoder Using Look Ahead Method (K=3 to 7)		Proposed Bit Level Pipelined Digit Serial Viterbi Decoder Method (K=3 to 7)	
	Frequency (MHz)	Average Power consumption(mw)	Frequency (MHz)	Average Power consumption(mw)
BMU	870	46	975.834	37
ACS		78.7		62.2
SMU		56.3		24
Viterbi decoder		192.1		142.6

Digit serial architecture is implemented in the FPGA device SPARTAN 3 xc3s400-5ft256. Table 3.2 summarizes the implementation details for Wordlength 8.

Table 3.2 Implementation Details for Wordlength 8

Parameters	Existing 2 Bit Level Pipelined Viterbi Decoder Using Look Ahead Method	Proposed Bit Level Pipelined Digit Serial Viterbi Decoder Method
Delay (ns)	2.35	0.801
No. of gate count	2115	1015
Memory devices	64	20

Table 3.3 Device Utilization Summary and power consumption for W=8 and W=32 for constraint length K=4

Logic utilization	Digit-serial for W=8	Digit-serial for W=32
Total number of slice register	358	850
Number 4 input LUTs	246	653
Number of occupied slices	286	623
Total number of 4 input LUTs	527	946
Number used as logic	246	653
Number of bonded IOBs	35	137
IOB latches	2	8
Number of GCLKs	1	8

Total equivalent gate count for design	6,522	13,755
Power Consumption (mW)	37	56

5. CONCLUSION

i. Viterbi decoder using digit serial unfolding concept is synthesized and implemented in Xilinx Spartan 3 FPGA for an unfolding factor J =2. The obtained results are compared with the existing 2 bit level pipelined look ahead technique and it is proved that the proposed method reduced power consumption by 25.76% with 10.09% increase in speed. The number of gates utilized is almost reduced to 2.04 times than that of the existing method. The limitation of this method is that as the unfolding factor J increases the complexity also increases. Also, the delay between the registers is to be balanced.

ii. In order to further reduce the delay and minimize the number of intermediate registers in Viterbi decoder, the SRL with wave pipelining concept is used to implement the Viterbi decoder. The design and simulation of the Viterbi decoder is at layout level with 65nm technology in Microwind. Power consumption of the wave pipeline work is reduced to 72.31% when compared to the existing single rail domino logic. Frequency of the wave pipeline design is obtained as 10 GHz, whereas the existing single rail domino logic frequency is of 1.43GHz. In view of delay, SRL with wave pipelining method has 3.08 times reduced delay with respect to the unfolding digit serial Viterbi decoder. Even though, the power consumption and delay are better in SRL with wave pipelining, it has its own limitation of high gate density

iii. The limitation of SRL with wave pipelining is trounced using GDI method. This method concentrates on reducing gate density and power consumption. GDI cell is similar in structure to that of CMOS logic. In this investigation, Viterbi decoder blocks are designed and simulated at transistor level in T-SPICE at 0.25□m technology. In a comparison of the average power consumption of the Viterbi decoder using GDI method with that of CMOS logic, the GDI method has shown better results. Power consumption is reduced by 29%, for a frequency of 25MHz and the area is reduced by 66%. ACS unit of the GDI based Viterbi decoder is compared with existing circuit styles like CMOS, static CMOS, domino logic and self resetting logic in terms of gate density and average power consumption. Comparison results have confirmed that GDI has almost 50% to 60 % less number of transistors and has minimum average power consumption.

iv. Based on asynchronous concept, Viterbi decoder is constructed using QDI templates PCHB and WCHB with a completion C-element. Performance of the asynchronous Viterbi decoder proved that there is 56.20% less power consumption when compared to that of synchronous design. Also, the power consumption has been reduced by 27% and it works at a frequency of 425MHz. The delay is 2.13ns with a transistor count of 16802.

v. Hence, the above four different VLSI architectures of the Viterbi decoder illustrated that the performances in terms of power, speed and area are improved when compared to the existing methods. With respect to the comparison results of the proposed four methods, it is found that GDI design has given better results in terms of power consumption, area and speed.

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