

Development of Transmitter chain in Direct RF Sampling board

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Abstract

Modern defence technology demands a reduced footprint with a better performance system to enhance operational efficiency, flexibility and survivability. This paper presents the development of a transmitter chain for radar systems implemented on a single silicon board using direct digital RF sampling. The integration of radar components onto a single silicon board represents a significant advancement in radar technology, offering potential benefits such as reduced size, cost and power consumption, as well as improved reliability and performance. The direct digital RF sampling approach enables high precision and flexibility in signal generation and processing, bypassing the traditional analog-to-digital conversion bottleneck. An RTL program has been developed to generate the precise timing signals required for radar operation. These timing signals act as a trigger to generate a pulsed CW signal, ensuring accurate and synchronized radar pulses [7].

Design methodology and architecture of the transmitter chain is discussed in this paper. Performance metrics such as signal fidelity, power efficiency, and operational bandwidth are evaluated through simulations and prototype measurements. The results demonstrate that the proposed transmitter chain achieves superior performance compared to conventional radars with a significant size reduction, making it a viable solution for next generation radar systems.

Keywords: RF, DDRFS, RTL program.

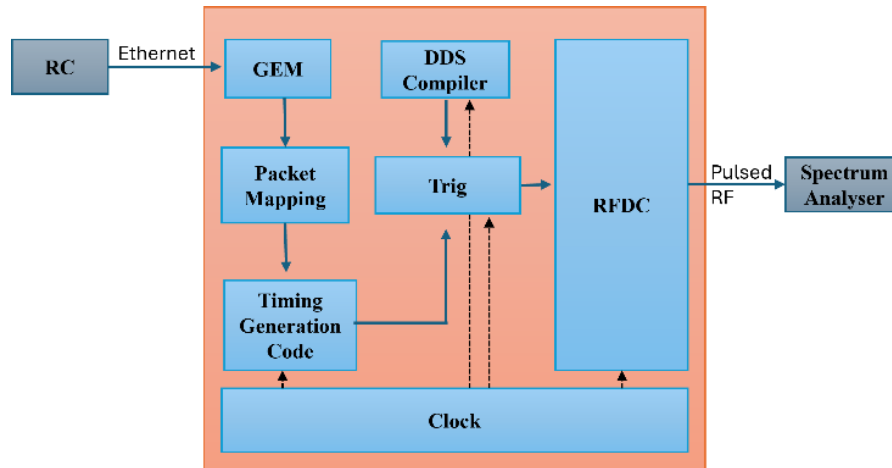
1. INTRODUCTION

- Precise timing and RF generation are critical in a wide range of applications, including radar systems, communication systems, and scientific instrumentation.
- Accurate timing control is essential for synchronization, data acquisition, and triggering mechanisms, which directly affect system performance and reliability.
- As the demand for higher resolution and faster data processing increases, traditional methods of RF signal generation face challenges in terms of flexibility, bandwidth, and timing accuracy.

- Direct digital RF Sampling (DDRFS) is an emerging method that addresses many of these challenges by digitizing RF signals directly at high sampling rates without the need for traditional analog down conversion stages.
- This approach leverages high speed analog-to-digital (ADC's), digital-to-analog (DAC's) and field-programmable gate arrays (FPGA's) to perform real time processing and generation of RF signals in the digital domain [3].
- DDRFS provides significant advantages in terms of spectral purity, frequency agility, and ease of integration into modern digital systems.
- This development is a step forward toward the use of DDRFS for RF signal generation, with an emphasis on using precise timing as a trigger for signal generation. By integrating timing control directly into the digital RF sampling process rather than integrating a separate timing generator sub-module to the old school RF transmission chain [4].
- This newer method of timing controlling the initialization of RF waveforms in a single board offers high degree of flexibility and precision in generation RF signal and better synchronization that can adapt to varying system requirements.
- The objective of this paper is to investigate how DDRFS can be employed to generate RF signal using precise timing triggers, analyse its performance, implementation challenges, and propose solutions to enhance the accuracy and minimize jitter.
- In this paper, (Section II) Architecture of radar pulsed signal generation is explained with the block diagrams. In (Section III) Brief about UDP packet mapping for timing generation in conjugation with timing generation code along with the result analysis. (Section IV) elaborates the timing generation required for radar transmission. (Section V) explains the trigger methodology used to trigger RF from the timing signals. In (Section VI & VIII) up-conversion process is explained followed by detailed clock configurations given to every RTL blocks (Section VII). (Section IX) Filters are used for single side band transmission. (Section X) actual test setup that was carried out and associated results drawn from the tests are discussed. The summary of the paper and future improvements is discussed in (Section XI).

2. ARCHITECTURE

Figure 1: Block Diagram

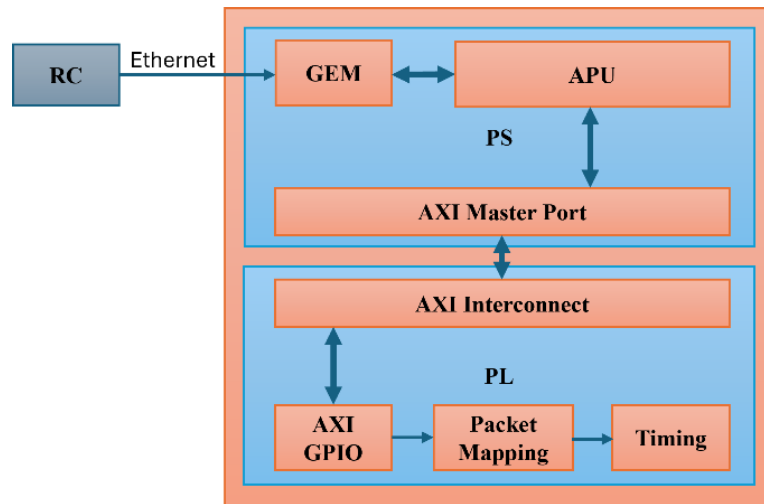


- Radar computer (RC) sends input data to the DDRFS board through ethernet as a UDP payload packet (fig 1).
- Payload contains all the information required to generate timings and RF. Payload data is extracted and mapped to the timing generation code module.
- DDS Compiler is used to generate the baseband signal [fig. 1]. Timing signal and baseband I and Q generator is passed through a programmed RTL block named as 'trig' (fig. 1) that functions as a trigger to the baseband I and Q data.
- Triggered value of I and Q is rowed as an input to the RF data converter (RFDC) which upconverts the baseband to the specified [5] C-Band carrier frequency. Resulting in the generation of C-Band pulsed RF signal.

3. UDP Packet Mapping

- The DDRFS board is interfaced with a radar computer that transmits UDP packets containing radar signal information's viz., "no. of pulses (NOP)", "pulse width (PW)", "dwell time (DT)", start of burst (SOB) and "transmit frequency (F_t)".
- A GEM portal on the DDRFS board facilitates the configuration of network parameters, including the IP address and port number, enabling seamless communication between the radar computer and the board.
- The incoming UDP packets are processed on the PS side, where the payload is extracted using bitwise operations.

Figure 2: Capturing UDP at PS and sending it to PL

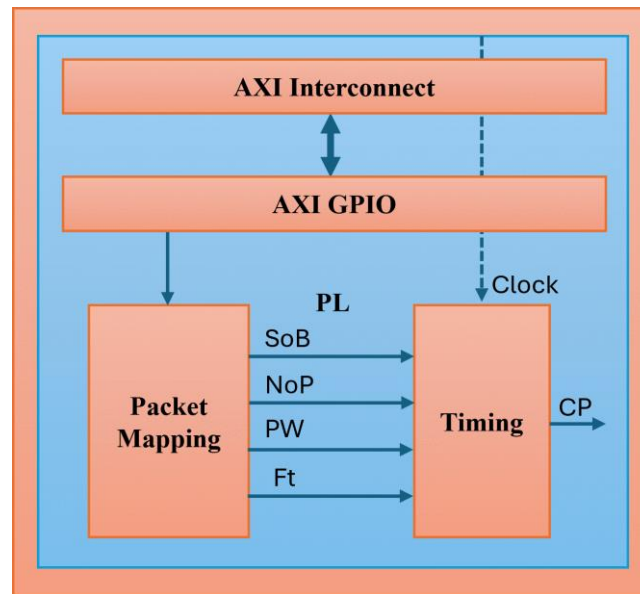


- The extracted payload from the UDP packets is forwarded to the PL side via memory mapped I/O, utilising the GPIO pins of the DDRFS board.
- This communication between the PS and PL side enables real-time processing and handling of radar data. The extracted payload is then mapped to a custom designed RTL module, which serves as an interface to the timing generation code module which is discussed in the next section.

4. Timing Generation

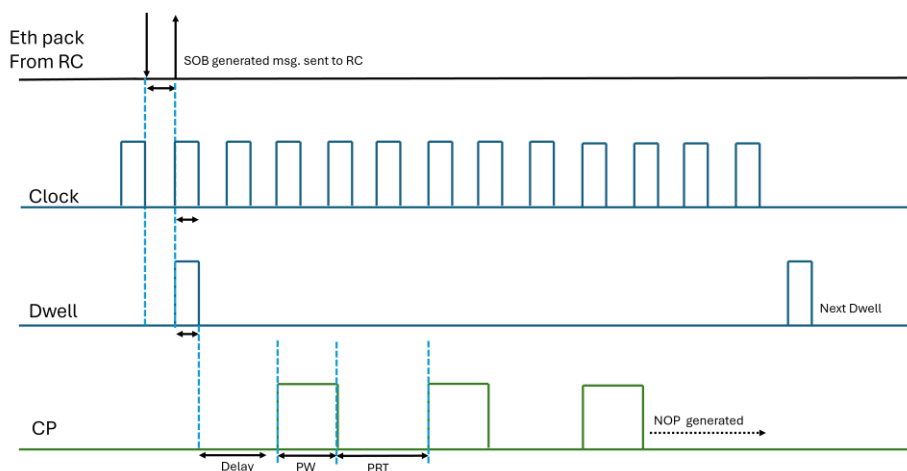
- Packet mapping RTL module [fig. 3] extracts the necessary information bitwise from the packets received. Following respective outputs are given as an input to the timing generation module [fig. 3]
- To generate the timing signal, a VHDL code for generating respective timing signals is written and the code is imported as an RTL module to the block diagram.
- Inputs and Outputs of the timing block is defined viz., “no. of pulses (NOP)”, “pulse width (PW)”, “dwell” and “transmit frequency (F_t)” are the inputs whereas “cover pulse (CP)” is one of the outputs of the timing block.

Figure 3: Timing Generation



- In the proposed system (fig. 3), a clock signal from the processing system (PS) is supplied to the timing generation module, which is responsible for generating the CP based on the information from the UDP packet (fig. 4).
- The generated CP is then utilized as an activation signal for the trig block (fig. 5), which governs the transmission of the I and Q data to the RF data converter (RFDC).
- The frequency information is also passed along and will subsequently be used to adjust the carrier frequency in the RFDC, as detailed in later section.

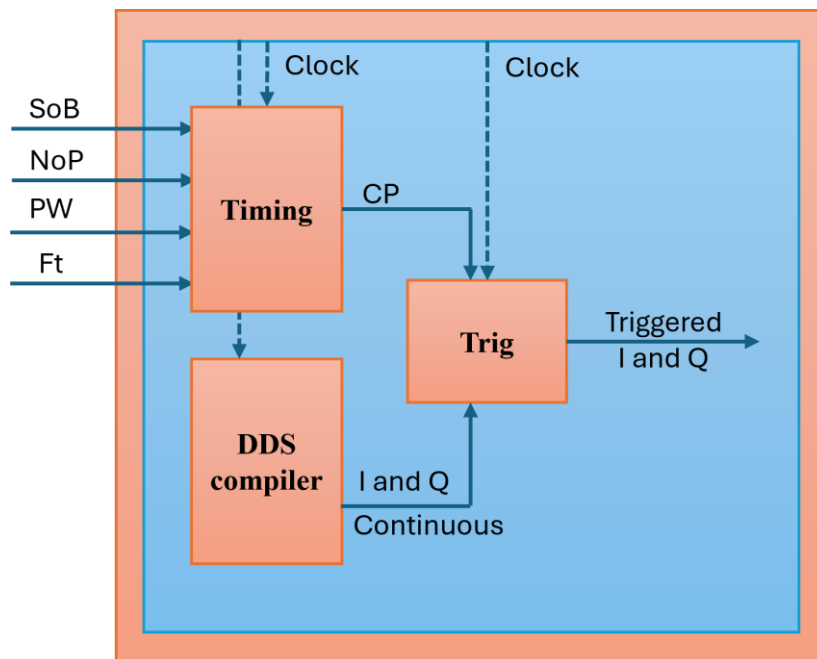
Figure 4: Timing Diagram



5. Trigger Mechanism

- DDS is utilized to generate a baseband signal in In-phase (I) and Quadrature-phase (Q) formats (fig. 5).
- The DDS block is configured to provide continuous I and Q samples at a rate synchronized to the clock expected by the RFDC within the system.
- This clock ensures that the generated baseband signal is compatible with the RFDC's sampling requirements.
- This continuous I and Q data is subsequently fed into a custom RTL block named trigger (fig. 5) before feeding it to the RFDC block.
- This module plays a crucial role in gating the baseband signal according to the cover pulse (CP) input it receives (fig. 5).
- Specifically, the Trig RTL block functions as a trigger, controlling the baseband signal output based on the rising and falling edges of the CP signal.
- By coordinating the signal generation with the CP input, the Trig RTL block enables the system to produce a pulsed wave (CW) signal.

Figure 5: Trigger mechanism block diagram



- This pulsed-modulated CW signal is given as an input to the RFDC block for the up conversion and digital to analog conversion.

6. Up Conversion & RF generation

- This part of implementation focuses on the RF data conversion where triggered digital I and Q data streams are input to the RFDC block. RFDC facilitates to configure NCO and DAC output during the run time.
- The sampling rate of the Digital-to-Analog converter (DAC) within the RFDC is governed by the carrier frequency requirement [1], while the DAC reference clock (fig. 6) is provided by the LMK chip, configured through a programmable interface on the DDRFS board.

7. Clock Configuration

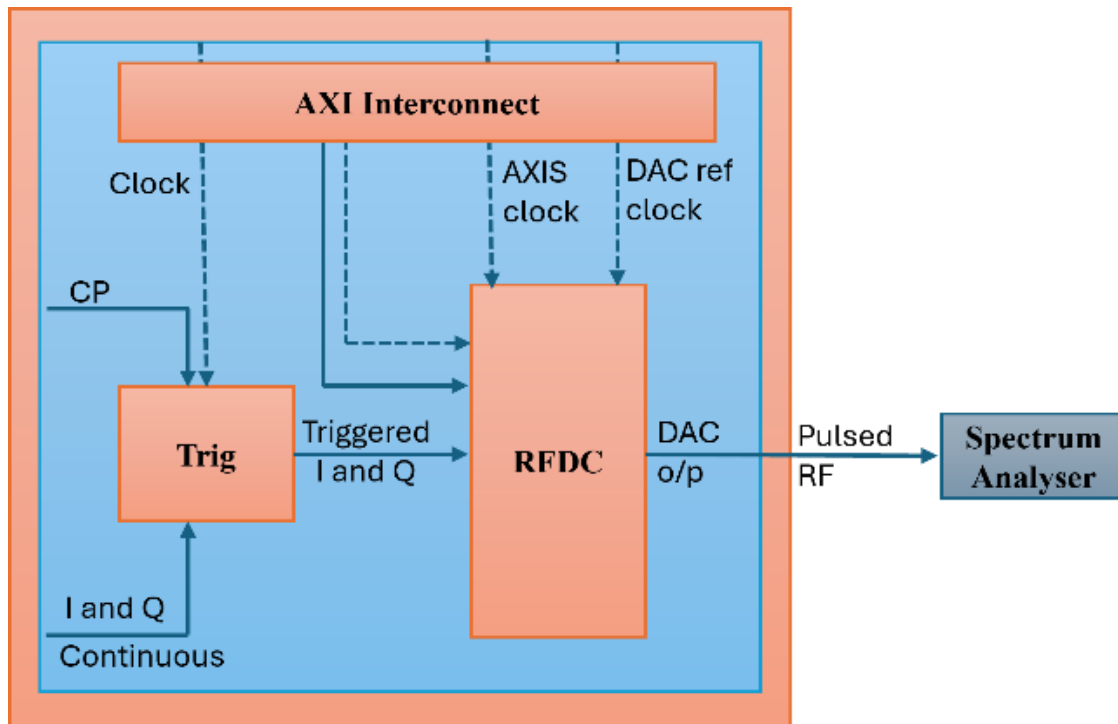
- The AXI4-Stream clock or AXIS clock (fig. 6) plays a critical role in the system by dictating the rate at which I and Q samples are fed into the RFDC.
- In this transmission chain, it is crucial to ensure clock synchronization across the RFDC, AXI4-Stream interface, Trig block and the DDS Compiler to avoid data loss or timing errors.
- All these components must operate on a common clock, determined by the required DAC's sampling frequency, interpolation factor, and the number of samples per data stream.
- The relationship between the system clock and the data flow can be defined as follows [2]:

$$F_s = I \times N_s \times F_{AXI} \quad (1)$$

Where:

- F_s represents the sampling frequency of the DAC,
- I is the interpolation factor used in the system.
- N_s denotes the number of samples processed per clock cycle,
- F_{AXI} is the AXI4-Stream clock, which controls the rate at which data is provided to the RFDC.
- This (equation 1) illustrates the dependency between the clock rates and the key parameters of the RF system emphasizing the need for synchronization.
- For optimal performance, the reference clock provided to the DAC (fig. 6) must be configured to match the required sampling frequency.
- LMK chip is programmed via set of register configuration to generate the required reference clock to the DAC, ensuring that the system operates seamlessly under varying carrier frequency.

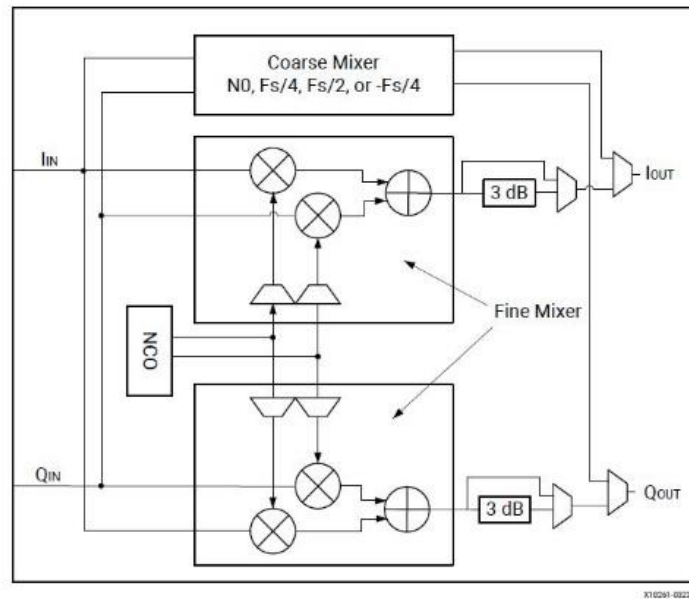
Figure 6: Integration of triggered I/Q data streams into RFDC using AXI4-Stream protocol and clocking synchronization.



8. Frequency Mixing

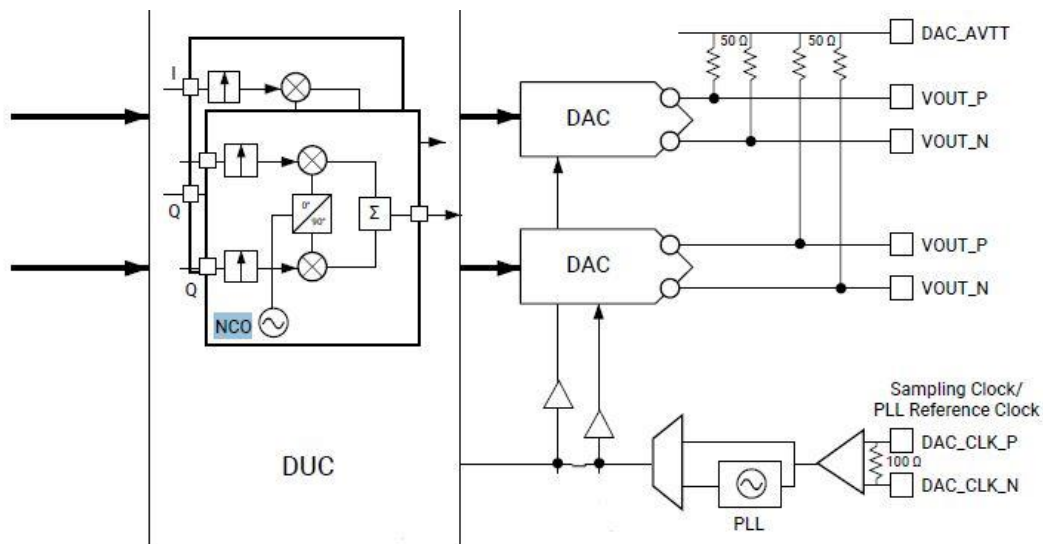
- The baseband I and Q data, triggered from the trig block, is first interpolated and then mixed with the output of the Numerically Controlled Oscillator (NCO) present on the DDRFS board [1].
- The NCO generates carrier frequency necessary for up conversion. This process enables the shift of the baseband signal to a higher frequency range through complex mixing. Mixing process is further elaborated in [1], and the block diagram is shown in (fig. 7).

Figure 7: I and Q complex mixing with NCO [1]



- The up converted signal is subsequently passed to the integrated DAC on the board (fig. 8), where the digital data is converted into an analog signal.

Figure 8: NCO to DAC architecture [1]



- The analog output is then analyzed using a spectrum analyzer (fig. 6) to verify the up-conversion process and assess the signal integrity at the carrier frequency.

9. Filters

- During the mixing process, the output contains several frequency components. Typically, Upper Sideband (USB) and Lower Sideband (LSB).
- For radar applications, using only one Sideband - either the upper or lower – is crucial for optimizing bandwidth and simplifying signal processing [6].
- For Single Sideband (SSB) transmission, digital IMR filters is used in this system. Following (fig. 9) appropriate Datapath mode is used to implement IMR in the system [1].

Figure 9: Datapath Mode [1]

Table 60: Datapath Modes

| Mode | Mode 1 | | Mode 2 | | Mode 3 | | Mode 4 | |
|----------------------------|------------------|-----------|--------------|-----------|---------------|-----------|------------|-----------|
| Short Name | Full Nyquist DUC | | IMR Low-pass | | IMR High-pass | | DUC-Bypass | |
| IMR x2 | OFF | | ON | | ON | | OFF | |
| Mix-Mode | OFF | ON | OFF | ON | OFF | ON | OFF | ON |
| Usable Bandwidth (F_s) | 0-0.45 | 0.55-0.95 | 0-0.2 | 0.8-0.95 | 0.3-0.45 | 0.55-0.7 | 0-0.45 | 0.55-0.95 |
| Reconstruction Filter | Low-pass | Band-pass | Low-pass | Band-pass | Low-pass | Band-pass | Low-pass | Band-pass |

Notes:

1. Usable bandwidth in this table is indicative and for reference only.
2. The maximum achievable RF-DAC rate in Mode 4 (DUC-bypass) is determined by the PL timing closure.
3. IMR High-pass mode shifts the original signal frequencies and inverts the spectrum.

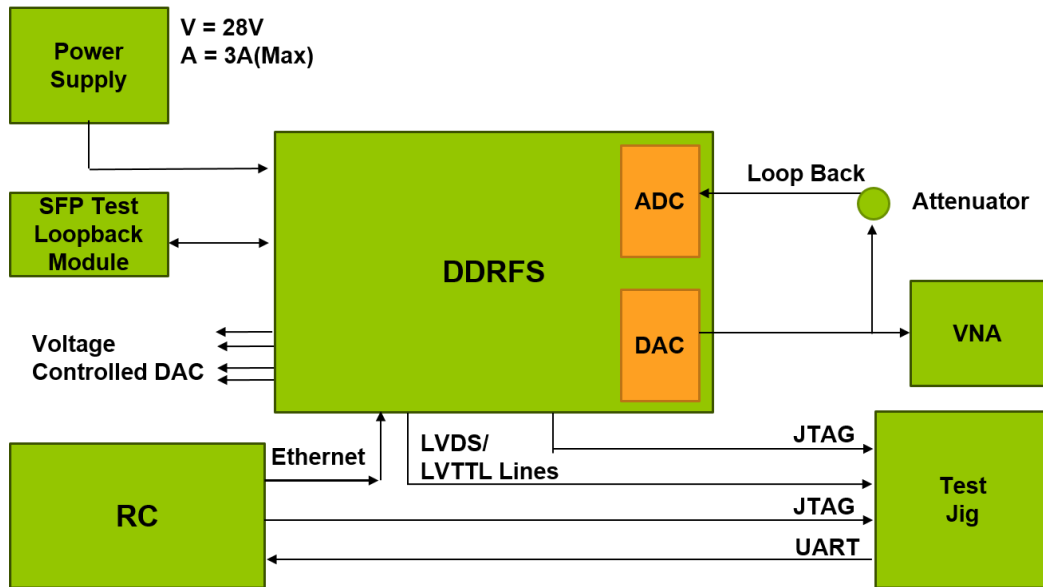
10. TEST SETUP & SIMULATION RESULTS

- Test setup was made with DDRFS board, and several tests were performed. Following test analysis and simulation are observed and discussed in this section

10.1. Setup

- The test aims to transmit UDP packets from the radar computer to DDRFS board, which will process the data, generate pulses, and allow monitoring using ILA and Vector Network Analyzer (VNA). The ILA will help analyze internal timing signals, while the VNA will analyze the board's RF performance. [Fig. 10]
- Setup Overview:
 - ✓ Power supply
 - ✓ Radar Computer / Laptop with RC GUI
 - ✓ Ethernet Cable
 - ✓ DDRFS Board
 - ✓ Laptop to monitor ILA/Test Jig
 - ✓ Attenuator 20dB
 - ✓ Vector Network Analyzer

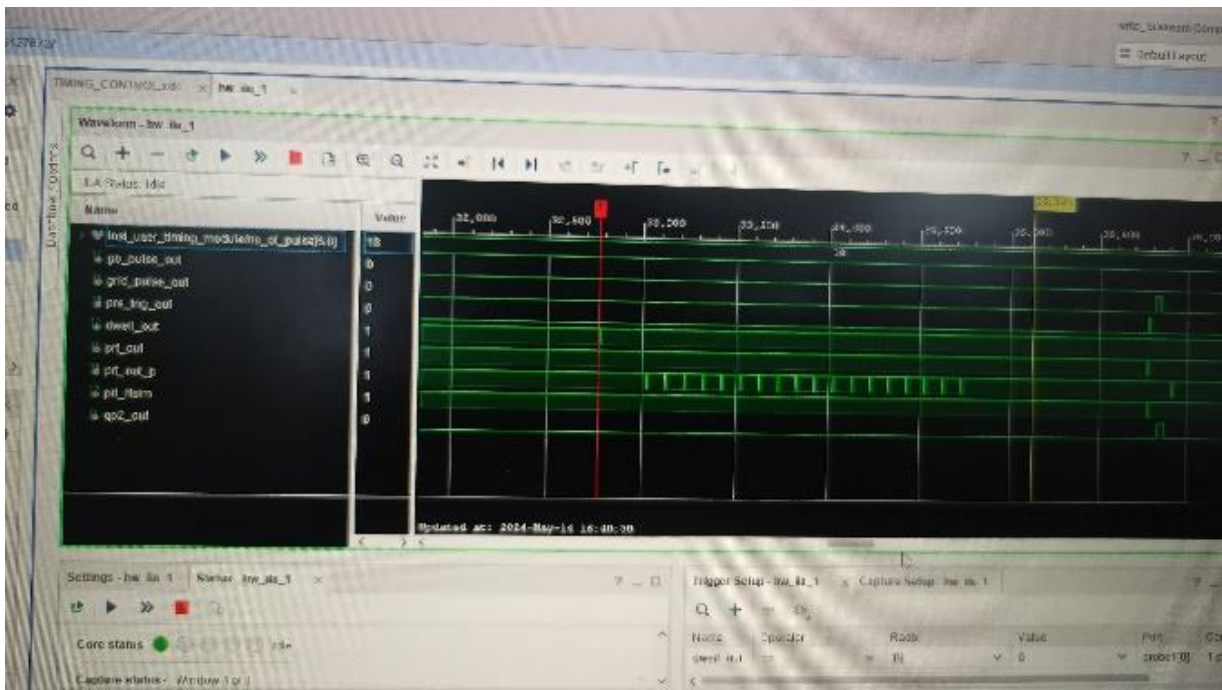
Figure 10: Test Setup



10.2. Timing analysis

- UDP packets were sent from RC and timing signals were monitored in ILA in vivado (fig. 11).
- Pulse width and PRT values of the timing signals are not mentioned on purpose due to confidential reasons as per the Official Secret Act, 1923.

Figure 11: Timing signal viz., Dwell, CP and other radar signals measured in ILA



10.3. Frequency analysis

- Spectrum analyser is used to measure the pulsed RF signal generated from the output of the DDRFS board. Calibrating cable loss and 20dB attenuator, Pulsed RF output power $\sim +9.7$ dBm.
- Following [Fig. 12] represents the RF signal measured in spectral domain with a span of 100MHz.
- Following [Fig. 13] represents the RF signal measured in time domain with a frequency span of 0MHz. Where Number of pulses (NOP), PW and PRT can be observed. Spot frequencies are hidden due to confidential reasons as per the Official Secret Act, 1923.

Figure 12: CW Pulsed RF signal monitored in VNA with a span of 100 MHz

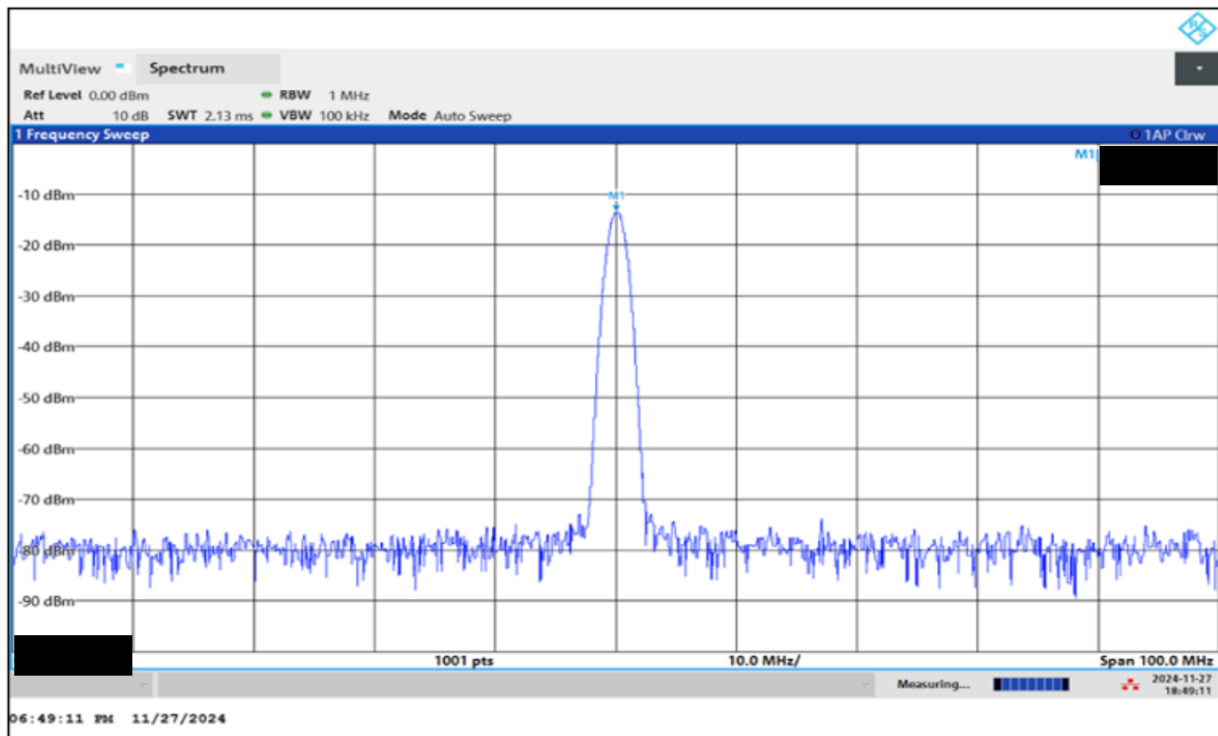
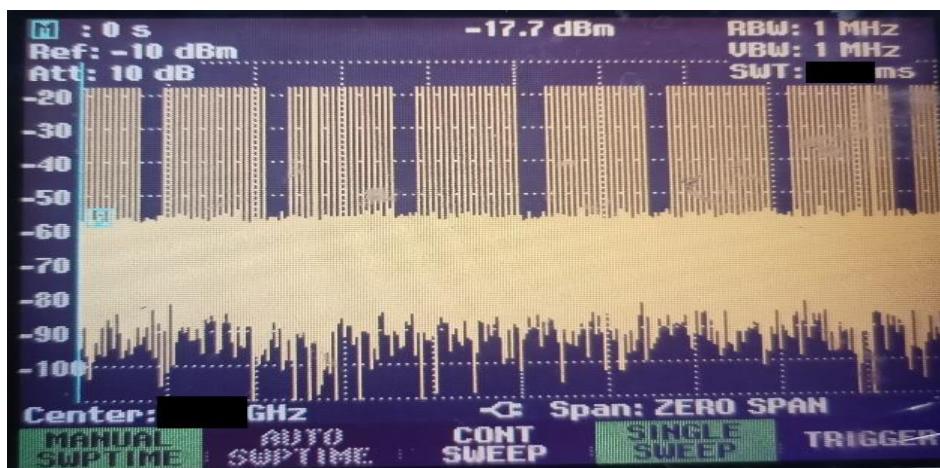


Figure 13: Pulsed RF signal monitored in VNA with Span of 0 MHz



10.4. Spurious/harmonics analysis

| Frequency serial no. | Frequency (MHz) | | Output power(dBm) | Spurious (dBc) | Harmonics (dBc) | |
|----------------------|--------------------------------------|--------------------|-------------------|----------------|-----------------|--------|
| | Set frequency | Measured frequency | | | 1st | 2nd |
| 0 | C- Band (15 spot frequencies) | | 9.5 | -80 | -57.8 | -60.5 |
| 1 | | | 9.76 | -80 | -57.76 | -63.6 |
| 2 | | | 9.89 | -80 | -61.19 | -67.72 |
| 3 | | | 9.59 | -80 | -65 | -80 |
| 4 | | | 9.31 | -80 | -65.11 | -80 |
| 5 | | | 9.23 | -80 | -65.78 | -80 |
| 6 | | | 9.13 | -80 | 60.53 | -80 |
| 7 | | | 9.47 | -80 | -61.47 | -80 |
| 8 | | | 10.25 | -80 | -60.75 | -80 |
| 9 | | | 11.03 | -80 | 59.63 | -80 |
| 10 | | | 10.5 | -80 | -59.9 | -80 |
| 11 | | | 10.4 | -80 | -60.1 | -80 |
| 12 | | | 9.9 | -80 | -59.6 | -80 |
| 13 | | | 9.3 | -80 | -59.2 | -80 |
| 14 | | | 9.3 | -80 | -59.3 | -80 |
| 15 | 9.9 | -80 | -61.1 | -80 | | |

10.5. Loop-Back Receiver Analysis

- Transmitted RF signal is looped back to the receiver. After down conversion, I and Q data is extracted and analysed in MATLAB [Fig. 15 and 16].
- Input power level = -50 dBm.

Figure 14: FFT of looped-back pulsed RF signal. Observation 1 and 2

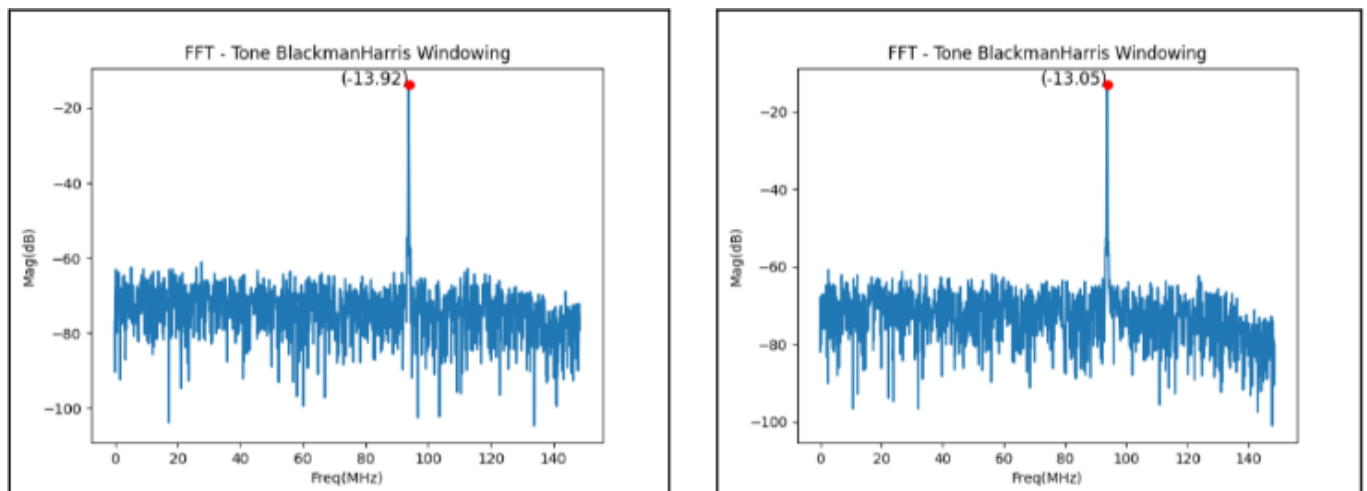
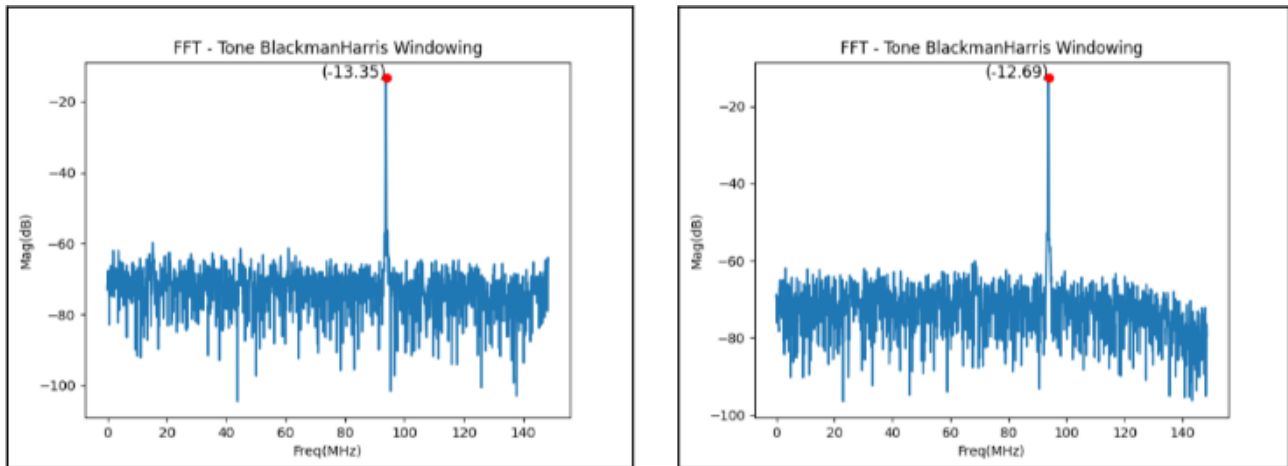


Figure 15: FFT of looped-back pulsed RF signal. Observation 3 and 4



11. CONCLUSION

The proposed design integrates timing generation, up conversion and pulsed RF generation in a single chip, offering a compact and efficient solution for modern radar systems. The advancements presented here highlights the potential of direct RF sampling technology in simplifying the transmitter architecture, improving performance and reducing the overall system complexity. This work have significant implications for the future of radar systems, offering potential improvements in both size and power efficiency. Future research could focus on refining the chip's capabilities to support higher frequency bands and advanced signal processing to further reduce the footprint and enhance the capabilities and versatility of radars.

12. ACKNOWLEDGEMENT

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13. AUTHORS' BIOGRAPHY



Piyush Bharti completed his B. Tech Degree in Electronics & Communication Engineering from NIT Jamshedpur in 2022. Since then, he has been working with Bharat Electronics Ltd, Bangalore in the field of Radars and Missile Systems. He is presently working as a Deputy Engineer in D&E-Missile Systems. His research areas include ESP-32 Microcontroller, Radar Analysis, Direct Digital RF Generation, Electronic Warfare and Decoy integration system.



Jaydip Jani received BE degree from Sardar Patel University in Electronics and Communication Engineering and M-Tech from IIT Delhi in Communication Engineering. He is presently working as Manager in Sonar systems group at Product Development and Innovation Centre (PDIC) of Bharat Electronics Limited, Bangalore. His research interest includes Electronic Warfare Systems, Image and Video Processing, Signal Processing, Radar Signal Processing, Sonar Signal Processing and AI & ML.



Raghavendra N A was born in Bangalore, Karnataka on July 3, 1990. He received his B. Tech Degree in Electronics & Communication Engineering from R.V college of Engineering, Bangalore in 2012. M. tech from IITM in Communication and Signal processing. Since then, he has been working with Bharat Electronics Ltd, Bangalore in the field of Radars and Missile Systems. He is presently working as a Deputy Manager in D&E-Missile Systems. His research areas include Radar Data Signal Processing, Electronic Warfare and SAM system integration. He has published papers at various international conferences. He has received 'Best Paper Award' in BEL Professional Paper Presentation.



R L Dodamani completed his B.E (E&C) from Karnataka University, Dharwad. Since July 1997, he has been working with Bharat Electronics Ltd, Bangalore in the field of receiver and signal processing systems for Radar projects. His major contributions include the development of receiver system for tracking radar & signal processing for weapon system tracking and surveillance radars. He is presently working as Additional General Manager (AGM) in D&E-Missile Systems. His interests include system integration of control centre, phased array radars and missile systems. He is a recipient of BEL R&D Excellence Award.

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