Advancing Research in Semiconductor Devices and Materials

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Abstract

Semiconductor devices and materials form the technological foundation of modern electronics, enabling advancements in computing, communication, energy, and intelligent systems. As conventional silicon-based complementary metal–oxide–semiconductor (CMOS) technology approaches fundamental scaling, power, and thermal limits, the need for innovative materials, architectures, and integration strategies becomes increasingly critical. This study provides a comprehensive overview of emerging trends in semiconductor research, encompassing advanced materials such as III–V compounds, germanium, and two-dimensional (2D) materials; novel device architectures including FinFETs, gate-all-around (GAA) transistors, and tunnel field-effect transistors (TFETs); and fabrication, characterization, and reliability considerations. The work further explores heterostructures, quantum and neuromorphic computing implications, simulation and data-driven design methodologies, and cross-cutting challenges related to power management and scalability. Ethical, environmental, and economic dimensions of semiconductor innovation are also examined. The analysis highlights that sustained progress in semiconductor technology requires interdisciplinary collaboration, integration of emerging materials, advanced modeling frameworks, and sustainability-oriented design approaches to meet future technological and societal demands.

Keywords: Semiconductor devices; CMOS technology; Two-dimensional (2D) materials; Heterostructures; FinFET; Gate-all-around (GAA) transistor; Tunnel FET (TFET).

1. Introduction

The complementary metal-oxide-semiconductor (CMOS) technology platform constitutes the backbone of the contemporary electronic industrial ecosystem. As the quest for continuous performance and power efficiency improvement faces critical scientific and technological challenges, a broad operational spectrum at the semiconductor-device and systems levels emerges as the most promising avenue for sustaining future advances in silicon–complementary metal-oxide-semiconductor (CMOS)-based electronics (Celano et al., 2024).

This work advances research in semiconductor devices and materials by providing an integrated perspective on the key scientific and technological challenges that shape the present environment. The accompanying collection features manuscripts that tackle the core challenges, which include

semiconductor materials, heterostructures, quantum and neuromorphic devices, scaling, reliability, fabrication, characterization, simulation and modeling, energy efficiency, and sustainability. A comprehensive overview identifying these aspects at the interface and cross-section of semiconductor-device and materials research is established.

Detailed accounts addressing each challenge appear alongside the overview, followed by consideration of emerging applications, simulation and performance keep, and acknowledgement of societal concerns.

2. Fundamentals of Semiconductor Physics

Semiconductors are essential materials for diverse, advanced electronic and optoelectronic devices. Along with dielectrics and metals, they form the fundamental building blocks of all electronic systems. Almost all commercial semiconductor devices are based on silicon (Si) or SiGe, GaAs, and GaN integrated on silicon or SiGe substrates. This section summarizes the structure and carrier statistics of semiconductors, the physical processes of recombination and transport and their models, and the modeling of the various device structures.

Semiconductors can be classified either by their bandgap or by the temperature dependence of their conductivity. The bandgap differentiates insulators (> 5 eV), semiconductors (0.5–5 eV), and metals (< 0.5 eV). The conductivity of semiconductors increases with temperature, in contrast to metals, where conductivity decreases with temperature. This bandgap and conduction property of semiconductors is exploited in all the semiconductor devices. (Bernardi et al., 2017)

3. Materials for Advanced Semiconductors

Advanced semiconductor devices enable novel functionalities to meet consumer demands for advanced computing, low-power solutions, and information security. Novel semiconductor materials, device architectures, and process technologies are essential for continued performance improvement. Traditional silicon technology faces significant material and performance limitations leading to device slowdown and saturation. The external quantum efficiency (EQE) of GaN-based light-emitting diodes (LEDs) remains below 30% even after significant research efforts. To address the limitations in silicon technology, several advanced materials are actively investigated for beyond-silicon devices. Silicon-based materials remain one of the most explored options because of the maturity of complementary metal–oxide semiconductor (CMOS) technology. III–V and germanium materials have received extensive attention because of their high mobility and compatibility with silicon technology. Two-dimensional (2D) materials have drawn great interest due to their unique properties and atomically thin nature that enable novel channels and integrated heterogeneous architecture with silicon technology (Bernardi et al., 2017) ; (Mark Spearing, 2003).

4. Device Architectures and Performance Metrics

The device architectures MOSFETs, FinFETs, GAA, and Tunnel FETs—and their performance metrics characterize semiconductor technologies. The mobility and drive current benchmarking conclusions

remain valid across the four architectures. Innovative concepts such as the 2D Material Transistor and the Memristive Device open the avenue to additional semiconductor technologies.

Electrons are the majority carriers since they are easily injected into the conduction band from the source. To quantify the speed of a device, the extraction delay is defined as depends on the extracted drain current and the supply voltage. Semiconductor technologies are judged using four indicators: (i) Drain Current, (ii) Extraction Delay, (iii) Subthreshold Slope, and (iv) Power, increasing importance are placed on power consumption for 3D integration in the future semiconductor technologies.

Data provided in (Lanza et al., 2020) allow comparison of emerging materials with those used worldwide at temperature above 300 K. Many two-dimensional materials cannot be deposited over the existing semiconductor before 300 K. A lower-limit temperature of 40 K can be anticipated for DyS-DSi-Si close-loop heterostructures. Combined with a 300 K-anchored 2D materials library and four-dimensional atomic-microstructure visualizers indicate that the DyS-DSi-Si GAA transistor counts as world-first front-end.

Memristive devices demonstrate Madison-WWT Comigration–Bridging Collection Accumulators and Memristive Vector Processors ease the transition toward computation-in-memory contains complementary-indicator about 1.1 / 1.4 mW / mm.^2 Energy/Area. Power Consumption Advances deliver importance energy budgets not in Permanent stage remain for arriving conventional semiconductor technologies concern of 630 K/130°C.

5. Fabrication Techniques and Process Integration

The fabrication of semiconductor devices relies on a sequence of technique-specific processing steps, commonly referred to as 'unit processes'. The lifetime of technology nodes is largely dictated by the ability to execute additional processing steps without detrimental effects on device performance while also providing the flexibility required to innovate new device structures, materials, or technologies.

The equipment and materials employed in manufacture exert a considerable influence on the achieved performance. Process specifications and materials of choice, however, must align with the starting substrates and pre-defined flow sequences. The widespread adoption of modular tools for volumetric detachment of materials, rather than their overall removal, enhanced the incorporation of, and shaped, competitive third-generation technology guidelines.

Doping, which dominates frontrunner sophistication metrics, similarly implements only voltage excitation once structure and material sets are identified. Device structure and materials-based process topology topographies, especially at the nodes, further tighten the choice and acceptance for doping. Consequently, both deposition and topography-defining layers remain fundamental to all prospective routes into the terminal stage. (Moss, 2022)

6. Characterization Methods and metrology

Semiconductor device development requires characterization of materials and structures to understand performance, integrity, and degradation mechanisms (Celano et al., 2024). Optical, electrical, chemical, and structural characterization techniques provide insights at various levels. Each method is based on different physical phenomena, and understanding their capabilities, limitations, and complementary aspects enables a tailored selection for specific measurement needs (T.Postek, 1994). Electrical methods investigate the macroscopic behavior of semiconductors under external influences, emphasizing parameters such as carrier concentration and mobility. Structural characterization probes dimensions, geometries, and crystalline quality. Optical measurements allow non-destructive access to energy levels, materials, and crystalline quality, while chemical techniques assess impurity-related energy levels and elemental distributions (Perkowitz et al., 1994).

Electrical, chemical, optical, and structural approaches establish the performance of semiconductor materials and devices and are extensively employed for reliability-expenditure lifetime and device-degradation acceleration. Surface and bulk characterization defines the specifications of semiconductor devices, metrology of geometry, flow, and etching damage, and a better understanding of aperture, end silicide contact, and as-grown Epitaxial material. Standard electrical characterizations are conducted for cut BoD devices and continuously biased pro-fabricated devices. Electrical, morphological, and chemical techniques measure the contact lengths and contact leakage of insulator metal semiconductor devices. These measurements indicate that the controlling and exhibiting behaviours have minor dependence on the contact length. Contamination from ultra-vacuum and argon pre-sputtered devices is studied, exhibiting that fabrication causes negligible device-performance degradation. Recovery in current ratio on the preparation and pre-sputtering is about ten times. The appreciable flexibility of an ultra-thin wafer for in-situ measurement and the adapted device structures for low-speed and miniaturization promote fuller device characterizations.

7. Reliability, Degradation Mechanisms, and Lifetime Prediction

Reliability remains a critical aspect of semiconductor devices that manufacturers face when touting the advantages of their products. Many degradation mechanisms exist, and lifetime prediction and characterization remain crucial topics in both the academic and industrial arenas. Increased reliability and lifetime advantages drive new semiconductor devices that pursue novel materials, heterostructures, and two-dimensional materials. These new flavors of semiconductor devices should also follow material and device architecture formation literature. Such importance warrants inclusion in advancing the topic of semiconductor devices.

Current semiconductor devices such as metal-oxide-semiconductor field-effect transistors (MOSFETs) and complementary metal-oxide-semiconductor (CMOS) have a long and reliable lifetime under continuous operation, acceleration tests, and temperature stress for monitoring through the industry. Existing accumulated knowledge on reliability system devices remains compatible with the evolution of semiconductor devices worldwide. New accelerated test methods for characterizing and determining degradation mechanism material and devices continue to emerge in tandem with accelerating development efforts at the material level (Alexander Karl, 1970).

8. Emerging Materials and Heterostructures

Efforts to pursue channel materials beyond conventional semiconductors seek to leverage the remarkable properties and heterostructuring capabilities of low-dimensional semiconductors. Consequently, two-dimensional (2D) materials and their heterostructures remain at the forefront of exploration. 2D materials have been extensively investigated as channel materials in future electronic devices because they provide atomically thin channels, enhancing electrostatic control while concurrently mitigating short-channel effects (Liu et al., 2019). Moreover, such materials can be stacked to form device architectures that exploit band engineering through 2D heterostructures. Tunneling field-effect transistors (TFETs) based on van der Waals insulator layers like hexagonal boron nitride (hBN) and transition metal dichalcogenides (TMDs) with large band gaps circumvent undesirable pinholes and defects. A TFET featuring a $SnSe_2/WSe_2$ heterostructure demonstrates a subthreshold swing of 80 mV/decade and an on/off current ratio greater than 10^6. Furthermore, memory devices employing 2D heterostructures including a programmable memory with $MoS_2/hBN/grapheme$ achieve on/off ratios exceeding 10^9 while exhibiting repeatable programming, erasing, and reading cycles via tunneling effects and asymmetric potential drops. The integration of ferroelectric insulators such as $CuInP_2S_6$ onto MoS_2 enables nonvolatile memory with stable ferroelectric hysteresis. In optoelectronics, 2D materials stand out because of their broad response spectrum, mechanical flexibility, and strong light–matter interactions.

9. Quantum and Neuromorphic Computing Implications

New paradigms in computing are revolutionizing traditional semiconductor device architectures, creating new requirements for the materials used. Quantum and neuromorphic computing draw inspiration from the structure and operation of systems and circuits found in Nature, as well as from nonlinear dynamics. Quantum computers continue to evolve, and implementations based on superconductors and atomic systems already exist. Additional architectures, such as those based on silicon, are under development but remain in the earlier stages of implementation limiting their near-term impact. New materials that enable the fundamental requirements of the silicon electron spin qubit have emerged. Recently, the spin qubit architecture has re-emerged as a competing and complementary candidate. For a solid-state spin qubit to emerge as a competitive candidate, materials that strongly couple to the spin state but avoid qubit-to-qubit crosstalk are needed. The spin–orbit interaction vanishes in materials with spatial inversion symmetry, and materials that can accommodate a larger and more versatile family of quantum defects—such as 2D semiconductors or wide-band-gap multi-valency systems—represent a key direction to pursue.

Another avenue for effort within quantum computing is the implementation of topological quantum computing, where the protected information is encoded in a non-abelian braiding of Majorana modes. Devices that can manipulate and detect non-abelian braiding are necessary. Quantum topological neuristors based on 2D topological insulators have been proposed. Quantum topological devices improve both reprogrammability and pulse operation speed, acting as a bridge between quantum and neuromorphic computing. A topological pathway for drug discovery based on a Quantum–Cl52d04fe8-9d6f-47d6-94ce-917a08faa76fcal Hybrid model has also been explored.

The second emerging computing paradigm, neuromorphic computing, draws from models of the brain's structure and operation to perform complex information processing and spatio–temporal pattern recognition tasks. Such systems use spiking or continuous transistors and can be equipped with memristors (S. Assi et al., 2023). Quantum neuromorphic systems leverage the power of quantum processing to dramatically increase the complexity of problems that can be solved while reducing the time to solution. The dynamical regimes of quantum neuromorphic systems must be expanded, allowing longer and more complex tasks to be performed. Emulations based on quantum topological systems can help better understand and increase their capacity. Quantum topological neuristors based on 2D quantum topological insulators have been proposed that act as synapse-like devices. The large energy gap and high mobilities associated with these materials enable ultra–low–energy data processing. Such devices are capable of efficient learning, re-learning, and forgetting.

10. Simulation, Modeling, and Data-Driven Design

Continuous technology scaling has rendered advanced semiconductor devices increasingly complex, raising the now prescient question of whether further reductions in device dimensions can continue to augment performance. Simulation, odelling, and data-driven design play an essential role in elucidating the odelling of semiconductor devices and estimating their potential. Technology computer-aided design (TCAD) serves the critical function of predicting the impacts of geometry, materials, and processing on electric characteristics; the design of experiments constitutes an additional tool for optimizing engineering parameters and driving process improvements. Effective TCAD relies on compact models that provide the required electrostatic, charge, and thermal information to circuit simulators without undue computational burden. Enhanced understanding of different materials and architectures promotes the development of new devices capable of meeting future performance demands.

Simulators based solely on first-principles approaches, including quantum mechanical models, multi-carrier Monte Carlo methods, and heat transport equations, are inherently limited by their overly simple representations of physical systems. Nevertheless, they facilitate the assessment of specific physics and phenomena and enable the a posteriori calibration of more general models. Meanwhile, data-driven methods involving machine learning and statistical analysis can serve as alternatives to analytical compact models, yet they too remain prone to significant challenges, with reproducibility, validation, and uncertainty quantification frequently remaining unaddressed (S. Lundstrom, 2015).

11. Cross-Cutting Challenges: Power, Thermal Management, and Scalability

As MOSFET dimensions shrink below the 10-nm node, improvements in performance, power, and scaling become exceedingly challenging (K. Pradhan et al., 2024). Power-sharing opportunities also diminish with circuit area reduction, and thermal designs grow more intricate, emphasizing electrothermal interactions. Covalent and van der Waals heterostructures enable exploration of additional materials and architectures to address these issues. Hybrid semiconductor materials systems can enhance local device performance improvement without altering the overall architecture or technology.

Packaging solutions for advanced semiconductor devices are generally divided into interposers, chiplets, multi-chip modules, and fan-out technologies. All of these options enable the implementation of new R&D and technology co-optimization.

Alternate/complimentary packaging technology such as FoWP is also already allowing technology/die partitioning within a substrate base. This helps that die can be process compatible isolation schemes allow flexibility such as attaching using max T allowed with dielectrics.

Alternately new embedded multiple field modules embedded to allow for odelling-sized chips disaggregated permitting wafer scale still across either disaggregated on or co-packaged.

12. Ethical, Environmental, and Economic Considerations

The semiconductor industry must address environmental, safety, and health threats associated with materials used in their products (Mullen & A. Morris, 2021). Developing universally accepted guidelines for assessing these challenges is difficult due to the industry's continual technological innovation, changing processes, and varying chemical usage. There are no standardized methods for evaluating sustainability or selecting low-impact materials. Operating within safe environmental boundaries is essential to prevent irreversible chemical effects, yet no comprehensive global assessment method exists. The industry relies on emerging techniques and principles like green chemistry to improve sustainability.

Guidelines and methodologies for environmentally benign technology development are needed despite successes in reducing the environmental footprint of semiconductor processes (Somani, 2007). Evaluating environmental, safety, and health impacts early in research and development is vital. Environmental, safety, and health constitute a critical axis alongside performance and cost, and quantifying environmental parameters for new and existing technologies enables better decision-making. Such issues must be integrated into the development process. Focusing on environmental, safety, and health parameters early offers an advantage to the industry and benefits the environment.

13. Conclusion

Advances in semiconductor devices and materials have enabled remarkable achievements in electronics, lighting, solar energy, and communication. Continued scaling of silicon complementary metal-oxide-semiconductor (CMOS) technology is hampered by physical, technical, economic, and realization limits. The International Technology Roadmap for Semiconductors has identified the need for innovation in materials and device concepts beyond Si technology alternatives to meet semiconductor industry needs and societal demands for improved functionality, performance, and energy efficiency (Bernardi et al., 2017).

Considerable progress has been made toward overcoming these challenges, yet significant gaps remain in understanding device operation, fabrication limits, and intrinsic performance; data-driven exploration of new materials, structures, and processing conditions; power, thermal, and reliability challenges; and their ultimate applicability to sustainable designs. Addressing such gaps and pursuing emerging scientific opportunities—2D materials and heterostructures; quantum, neuromorphic, and magneto-

electronic computing; and novel simulation, odelling, and machine-learning-based design techniques—promise to enhance research capability and accelerate the advancement of semiconductor science, devices, and systems concerned with information exchange, processing, storage, and sustainability (Lanza et al., 2020).

References:

1. Celano, U., Schmidt, D., Beitia, C., Orji, G., V. Davydov, A., & Obeng, Y. (2024). Metrology for 2D materials: a perspective review from the international roadmap for devices and systems. ncbi.nlm.nih.gov

2. Bernardi, M., Ataca, C., Palummo, M., & C. Grossman, J. (2017). Optical and Electronic Properties of Two-Dimensional Layered Materials.

3. Mark Spearing, S. (2003). MEMS Materials and Processes: a research overview.

4. Lanza, M., Smets, Q., Huyghebaert, C., & Li, L. J. (2020). Yield, variability, reliability, and stability of two-dimensional materials based solid-state electronic devices. ncbi.nlm.nih.gov

5. Moss, D. (2022). Fabrication methods for integrating 2D materials.

6. T. Postek, M. (1994). Critical Issues in Scanning Electron Microscope Metrology. ncbi.nlm.nih.gov

7. Perkowitz, S., G. Seiler, D., & M. Duncan, W. (1994). Optical Characterization in Microelectronics Manufacturing. ncbi.nlm.nih.gov

8. Alexander Karl, E. (1970). Unreliable Silicon: Circuit through System-Level Techniques for Mitigating the Adverse Effects of Process Variation, Device Degradation and Environmental Conditions..

9. Liu, Y., Zhang, S., He, J., M. Wang, Z., & Liu, Z. (2019). Recent Progress in the Fabrication, Properties, and Devices of Heterostructures Based on 2D Materials. ncbi.nlm.nih.gov

10. S. Assi, D., Huang, H., Karthikeyan, V., C. S. Theja, V., Merlyne de Souza, M., Xi, N., Jung Li, W., & A. L. Roy, V. (2023). Quantum Topological Neuristors for Advanced Neuromorphic Intelligent Systems. ncbi.nlm.nih.gov

11. S. Lundstrom, M. (2015). Computational Electronics for the 21st Century: Reflections on the Past, Present, and Future.

12. Pradhan, D., C. Moore, D., Matt Francis, A., Kupernik, J., Joshua Kennedy, W., R. Glavin, N., H. Olsson, R., & Jariwala, D. (2024). Materials for High Temperature Digital Electronics.

13. Mullen, E. & A. Morris, M. (2021). Green Nanofabrication Opportunities in the Semiconductor Industry: A Life Cycle Perspective. ncbi.nlm.nih.gov

14. Somani, A. (2007). Manufacturing of three dimensional integrated circuits.