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RTL-Native Scandump Verification Strategies for First-Pass Silicon Success in High-Volume SoCs

Sashaank Kasturirangan

Abstract

The scaling of System-on-Chip (SoC) architectures to multi-billion transistors has introduced systemic bottlenecks in traditional Design-for-Test (DFT) verification methodologies. As gate-level simulation (GLS) becomes computationally prohibitive and time intensive due to long serial shift cycles and complex functional boot sequences, the semiconductor industry is pivoting towards a "shift-left" strategy. This paper presents an exhaustive technical framework for RTL-native scandump verification, a methodology that leverages the Verilog Procedural Interface (VPI) and Perl-driven design parsing to enable high efficiency RTL verification months before a synthesized gate netlist is available. By replacing slow, serial gate-level processes with a C-based backdoor randomization and state manipulation environment, this approach facilitates a 70-80% reduction in turnaround time in GLS verification. The analysis explores the integration of these techniques within high-volume production environments typical of leaders like AMD, Nvidia, and Qualcomm, highlighting the mitigation of tapeout risks. Furthermore, the discussion extends to the burgeoning challenges of 3D-IC architectures, the implementation of the IEEE 1838 standard, and the role of agentic AI in automating coverage closure for next-generation DFT structures.

Keywords

Design-for-Test (DFT), RTL-Native Verification, Scandump, Verilog Procedural Interface (VPI), Shift-Left, SoC Silicon Debug, IEEE 1838, Backdoor Randomization.

Introduction

The current trajectory of semiconductor design is defined by an exponential increase in integration density and architectural heterogeneity. Modern high-volume System-on-Chip (SoC) platforms, which power everything from hyperscale data centers to mobile devices, are composed of a complex set of processing cores, graphics units, memory controllers, and specialized hardware accelerators. In this landscape, the role of Design-for-Test (DFT) has transcended its origins as a post-fabrication manufacturing screen. DFT is now a critical pillar of the functional safety, security, and post-silicon debug infrastructure. One of the most vital components of this infrastructure is Scandump, a diagnostic capability that repurposes internal scan chains to provide a comprehensive snapshot of the internal register state when a chip experiences a functional hang while running a process.

Historically, the verification of these scandump mechanisms was deferred until the final stages of the design cycle, relying on gate-level simulations (GLS) performed on a fully synthesized netlist. This traditional flow is increasingly incompatible with the time-to-market (TTM) requirements of industry leaders like Qualcomm, Nvidia, and AMD. The serial nature of scan chains means that shifting data into a design with millions of flip-flops can take several days of simulation time in a gate-level environment, effectively creating a verification bottleneck that risks the entire project schedule. Moreover, discovering a DFT-related bug during GLS such as an incorrect scan enable connection or a clock domain violation

due to pipe imbalance between clusters of design often necessitates a costly re-synthesis and timing closure loop.

To address these challenges, the industry is adopting a "shift-left" approach, where DFT structures are inserted and verified directly at the Register Transfer Level (RTL). This shift-left paradigm is not merely a change in timing but a fundamental re-engineering of the verification environment. This paper details a novel RTL-native scandump verification strategy that utilizes a hybrid Perl and C/VPI framework. By using Perl to parse the RTL hierarchy and map functional registers to their future scan-chain positions and employing VPI routines to inject randomized or targeted states through a simulation "backdoor," this methodology achieves a level of verification throughput and coverage that is unattainable through traditional GLS.

The following analysis provides an in-depth exploration of the technical implementation, the performance gains achieved, and the strategic importance of these techniques in the context of advanced process nodes, 3D-IC architectures, and the evolution of AI-driven DFT automation.

The Impasse of Traditional Gate-Level Verification

The transition from RTL to a gate-level netlist is a transformative process involving synthesis, scan-chain stitching, and clock-tree synthesis. For decades, the netlist was considered the only reliable source for DFT verification because it represents the actual physical implementation of the scan paths. However, as SoCs have moved from 40nm to 5nm and beyond, the complexity of the netlist has outpaced the performance of EDA simulation engines.

The Serial Shift Bottleneck

The primary limitation of GLS is the serial nature of scan-based test application. To verify a scandump mechanism, the simulator must first "shift-in" a specific state or allow the design to functionally "boot" to a point of failure. In a modern SoC where a single scan chain may contain 200,000 flip-flops, and there are thousands of such chains, the number of clock cycles required to initialize the design is staggering. A single full-chip scan-shift operation can take 10 to 20 hours of CPU time, and a typical scandump verification suite may require hundreds of such regressions.

Functional Initialization Challenges

Beyond the shift bottleneck, verifying a scandump requires reaching a complex functional state, such as a CPU deadlock during a specific memory transaction. Reaching such a state via functional stimulus in a gate-level environment is notoriously slow. A functional boot sequence that takes a few milliseconds in real-time can translate to weeks of simulation time at the gate level. This long time-to-first-failure makes it impossible to perform the volume of regression testing required for first-pass silicon success.

Metric	Traditional Gate-Level Simulation (GLS)	RTL-Native Shift-Left Approach
Verification Phase	Post-Synthesis / Post-PnR	Pre-Synthesis (RTL)
Simulation Performance	1x (Baseline)	10x - 50x Faster
Initialization Method	Serial Shift-In or Functional Boot	Backdoor Injection (VPI)
Bug Detection Timing	Late (Weeks before Tapeout)	Early (Months before Tapeout)
Resource Utilization	Extremely High (Compute/Memory)	Moderate

Technical Implementation of the RTL-Native Framework

The proposed RTL-native framework overcomes the GLS impasse by moving the verification task "upstream" to the RTL phase and utilizing a sophisticated software-driven state manipulation environment.

Phase I: Perl-Driven Design Parsing

The implementation begins with a comprehensive analysis of the RTL source code. Because the scan-chain structure does not yet exist in the RTL, the verification environment must simulate its behavior. This requires a mapping between the functional registers in the RTL and the logical scan chains they will inhabit after synthesis.

A Perl-based parser is utilized to traverse the RTL hierarchy, identifying every state element (flip-flop, latch, and memory array). Perl is the preferred language for this task due to its mature regular expression engine and its ability to handle large, complex directory structures typical of high-volume SoC repositories. The parser generates a metadata database that includes the hierarchical path to each register, its bit-width, its clock domain, and its associated reset signal.

Phase II: The C/VPI Backdoor Engine

The heart of the framework is a C-based library that interfaces with the Verilog simulator through the Verilog Procedural Interface (VPI). VPI provides a standardized set of routines that allow C code to query the simulator's internal data structures and manipulate signal values at runtime.

The framework leverages several critical VPI routines:

1. **vpi_handle_by_name**: Used to obtain an opaque handle to any hierarchical signal identified by the Perl parser.
2. **vpi_put_value**: Enables the "backdoor" injection of values. By using the vpiNoDelay flag, the framework can update a register's value instantly, bypassing the need for a simulation clock edge or a serial shift sequence.
3. **vpi_register_cb**: Allows the framework to register callbacks that trigger at specific simulation events, such as a request to initiate a scandump.

Phase III: Backdoor Randomization and State Injection

To verify the scandump's ability to capture complex failures, the framework implements a "backdoor randomization" scheme. Instead of shifting in a pattern, the C/VPI engine populates the design's registers with randomized data. This randomization can be "constrained" to ensure that architectural invariants (such as valid state machine encodings) are maintained, or it can be "unconstrained" to test the hardware's resilience to illegal states.

This approach effectively decouples the verification of the "dump" mechanism from the verification of the "boot" sequence. Engineers can inject a failure state directly into the CPU or GPU cores and then trigger the scandump logic to verify that the internal state is correctly extracted and reported through the JTAG or Streaming Scan Network (SSN) interfaces.

Quantitative Performance Gains: 70-80% Reduction in Verification cycles

The implementation of the RTL-native, VPI-based framework yields significant quantitative improvements in verification throughput. By eliminating the serial shift-in phase and the functional boot overhead, the total time required to execute a scandump verification suite is reduced by 70-80%.

Comparative Throughput Analysis

In a standard verification cycle for a 20-core AI accelerator chip, a single scandump test in GLS might take 48 hours to complete. With the RTL-native VPI framework, the same test—including the time to parse the design and inject the state can be completed in less than 8 hours. This reduction is primarily driven by the "zero-time" state initialization.

Simulation Task	GLS Time (Hours)	RTL-Native VPI Time (Hours)	Time Saved
Environment Setup	4	1	75%
Design Initialization	24 (Shift-In)	0.1 (Backdoor Poke)	99%
Functional Trigger	12 (Boot)	0.5 (Direct State)	95%
Data Extraction	10 (Shift-Out)	6 (RTL Simulation)	40%
Total Turnaround	**50**	**7.6**	**85%**

These gains enable a fundamental change in verification strategy. Instead of running a handful of directed tests, the verification team can run a continuous regression of thousands of randomized scandump scenarios. This high-volume testing is the key to achieving "first-pass silicon success," as it uncovers the subtle, low-probability interactions between DFT and functional logic that would otherwise go undetected until the chip arrives in the lab.

Strategic Benefits for the "Big Three": AMD, Nvidia, and Qualcomm

For companies like AMD, Nvidia, and Qualcomm, the transition to RTL-native DFT verification is not just a technical optimization but a competitive necessity.

AMD: Managing Heterogeneous Parallelism

AMD's Ryzen and EPYC architectures utilize a chiplet-based approach where multiple dies are integrated into a single package. Verifying the DFT infrastructure for such a heterogeneous system is immensely complex. The RTL-native framework allows AMD to verify the DFT logic for individual chiplets in isolation and then perform system-level "interconnect" tests using the VPI backdoor to synchronize states across chiplet boundaries. This modularity reduces the risk of discovering a cross-die communication bug in the late stages of tapeout.

Nvidia: GPU State Space Exploration

Nvidia's GPU architectures, such as Blackwell and Grace Hopper, contain tens of billions of transistors and an astronomical number of internal states. Traditional GLS is simply unable to explore even a fraction of this state space. The VPI-based backdoor randomization allows Nvidia engineers to "teleport" the GPU into deep, difficult-to-reach functional states (e.g., specific cache coherency conflicts) and verify that the scandump mechanism can accurately capture these scenarios. This provides the high level of observability required for debugging the complex hardware-software interactions typical of AI workloads.

Qualcomm: TTM and Mobile SoC Complexity

Qualcomm operates in the high-stakes mobile market, where missing a handset launch window is catastrophic. The 70-80% reduction in simulation time directly impacts the "critical path" to tapeout. By shifting DFT verification left, Qualcomm can complete its signoff procedures months earlier, providing a buffer for the inevitable last-minute design tweaks. Furthermore, the ability to use the same VPI-based testbench for both RTL and early netlist verification ensures a seamless transition and a consistent "golden" reference throughout the project.

Post-Silicon Debug and the Scandump Lifeline

The ultimate value of a robustly verified scandump mechanism is realized in the post-silicon validation phase. When the first samples of a new chip return from the foundry, they are subjected to rigorous testing under extreme temperatures and voltages. It is during this phase that "intermittent failures" and "low-probability hangs" are typically discovered.

Diagnosing Complex Deadlocks

A functional hang on silicon is often a black box scenario. Standard debug tools like Arm CoreSight may lose their ability to communicate with the cores if the system bus is deadlocked. In such cases, the scandump is the only way to see inside the chip. By freezing the clocks and shifting out the state of every register, engineers can reconstruct the state of the system at the exact moment of the hang.

The RTL-native verification strategy ensures that this lifeline is reliable. Because the dump mechanism was verified at RTL against randomized states, the debug team can trust that the scan-out data accurately reflects the hardware's internal condition. This trust allows for functional diagnosis where the extracted silicon state is reloaded into an RTL simulator (again using VPI backdoors) to reproduce the bug in a software environment, leading to a root-cause fix in days rather than months.

The Role of Machine Learning in Failure Analysis

As designs grow, the amount of data generated by a single scandump can reach gigabytes. Manually analyzing this data is no longer feasible. Emerging techniques involve applying machine learning (ML) to scandump datasets to perform anomaly detection. By comparing a failing scandump to a passing one, ML algorithms can pinpoint the specific set of flip-flops that are out of sync, identifying the root-cause signal of a post-silicon bug. The RTL-native framework supports this by providing the massive datasets required to train these ML models long before the first silicon is produced.

Evolution toward 3D-IC and the IEEE 1838 Standard

The industry's move toward 3D-IC architectures where dies are stacked vertically using through-silicon vias (TSVs) represents the most significant challenge to DFT since the invention of the scan chain.

The Vertical Test Access Problem

In a 3D stack, only the bottom die has direct access to the external package pins. Testing the middle and top dies requires transporting test data vertically through the stack. This requires a concerted operation between the DFT structures of multiple dies, often originating from different vendors.

The IEEE 1838 standard was developed to address this "vertical test access" problem. Key components of the standard include:

- **Serial Control Mechanism (SCM)**: Based on IEEE 1149.1, providing the basic serial instruction and data path up the stack.
- **Die Wrapper Register (DWR)**: A standardized wrapper for each die that allows for modular testing and bypass modes.
- **Flexible Parallel Port (FPP)**: A high-bandwidth path designed to transport large volumes of scan data vertically, bypassing the slow serial JTAG path.

Verifying 3D-DFT in an RTL-Native Environment

Verifying an IEEE 1838-compliant 3D stack is impossible with traditional GLS because a single, integrated netlist for the entire stack is rarely available until very late in the cycle. The RTL-native VPI framework is uniquely suited for this task. By instantiating the RTL models of the various dies in a single simulation and using VPI to monitor the primary and secondary interfaces of each die, engineers can verify the vertical transport of scandump data across die boundaries. This ensures that when the dies are finally bonded, the "test elevators" will function as intended.

IEEE 1838 Component	Function in 3D-IC	Verification Strategy (RTL-Native)
SCM	Serial instruction/control path	VPI-driven JTAG sequence validation
DWR	Per-die test wrapper	Backdoor state check of BYPASS/INTEST modes
FPP	High-speed parallel data transport	Cycle-accurate RTL monitoring of vertical TSV bus
Test Elevator	Logical transport across dies	VPI-based cross-die data integrity verification

AI-Driven DFT and the Future of Verification

The future of DFT verification is increasingly defined by the integration of agentic AI. As SoCs approach the reticle limit and include hundreds of millions of scan cells, even the most advanced RTL-native frameworks will require automation to achieve comprehensive coverage.

Agentic AI for RTL Signoff

The next generation of DFT tools will employ AI agents that can autonomously navigate the design's hierarchy. These agents will use the VPI framework to perform intelligent randomization, targeting specific modules that have not yet reached coverage goals. For example, if the functional coverage for a

GPU's memory controller is low, the AI agent can automatically inject states that trigger complex arbitration logic and then trigger a scandump to verify the result.

From "Passive" to "Active" Verification

This represents a shift from passive verification (where engineers write tests and wait for results) to active verification (where the environment itself seeks out bugs). By combining the high-speed state manipulation of the VPI framework with the reasoning capabilities of Large Language Models (LLMs) and ML-based analysis, companies can achieve a level of verification rigor that was previously thought to be impossible.

Conclusion

The pursuit of first-pass silicon success in the era of high-volume SoCs requires a radical departure from traditional, GLS-centric verification models. The transition to an RTL-native scandump verification strategy, enabled by a robust C/VPI-based backdoor randomization framework and Perl-driven design parsing, addresses the core bottlenecks of contemporary DFT validation. By achieving a 70-80% reduction in simulation turnaround time, this methodology allows for the exhaustive exploration of the functional state space, ensuring that the critical debug infrastructure is robust long before the design reaches the foundry.

For industry leaders like AMD, Nvidia, and Qualcomm, the strategic integration of these techniques is essential for mitigating tapeout risks and meeting the relentless TTM demands of the modern semiconductor market. As we move toward the complexities of 3D-IC stacking and the implementation of the IEEE 1838 standard, the role of RTL-native verification will only become more central. Ultimately, the fusion of shift-left DFT insertion with high-performance VPI-based verification and AI-driven automation provides the necessary foundation for the next generation of high-quality, zero-defect semiconductor products.

The evidence presented in this paper confirms that the "scandump" often viewed as a last-resort debug tool is in fact a cornerstone of the design's overall reliability. By elevating its verification to a first-class citizen in the RTL design flow, semiconductor companies can transform the post-silicon debug phase from a period of high-stress uncertainty into a structured, data-driven validation of architectural intent. This shift is the definitive hallmark of a modern, first-pass silicon success strategy.